

# Compal Confidential

DLID4 / D5

DIS M/B Schematic Document

Intel KabyLake U/KabyLake R Processor with DDR4

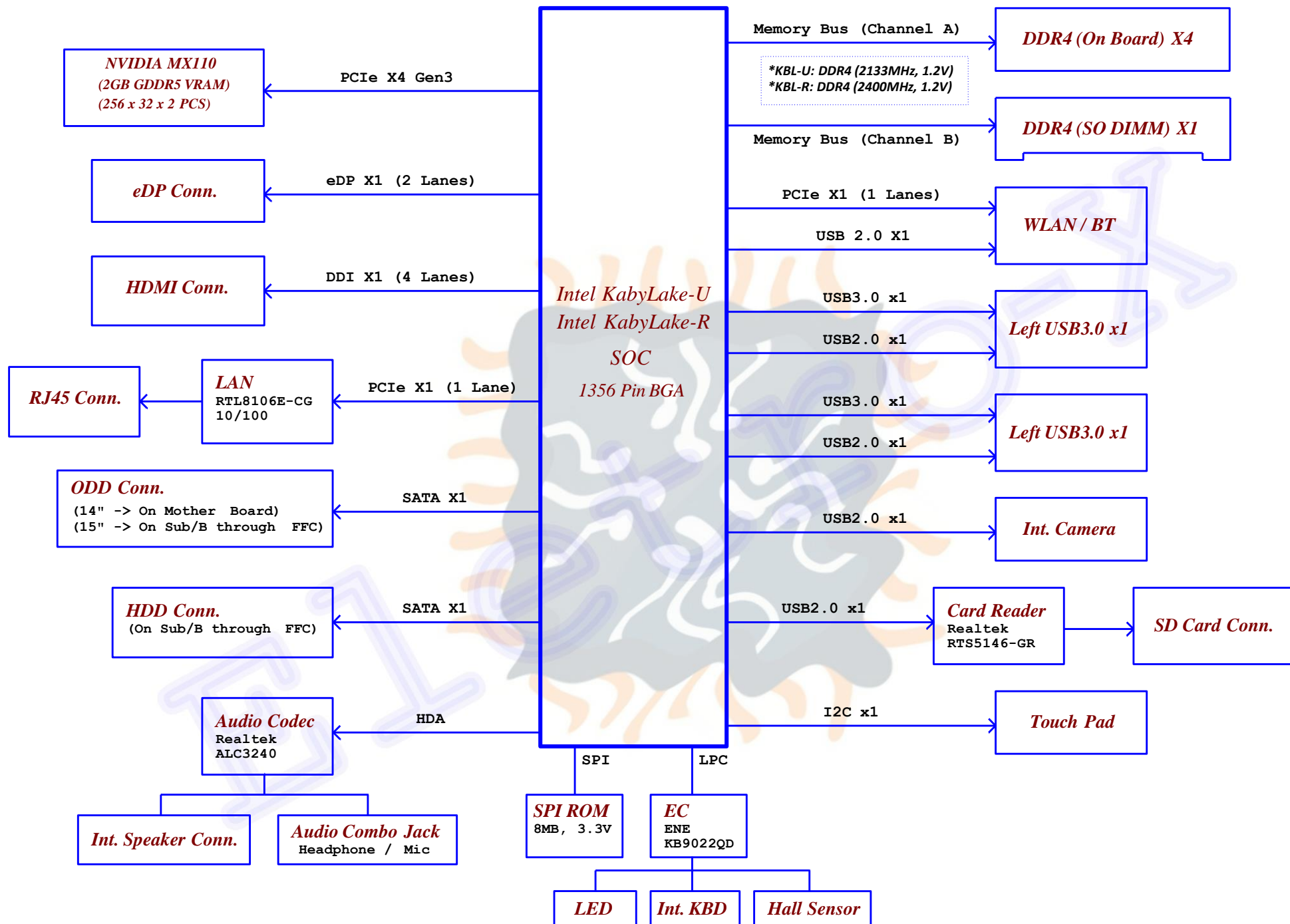
LA-G202P

2018-03-09

REV 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/03/09	Deciphered	2019/03/09	Cover Page	
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				Custom	LA-G202P
				Date:	Friday, March 09, 2018
				Sheet	1 of 1





**-PowerMap\_KBL\_DDR4\_Volume\_NON CS]**

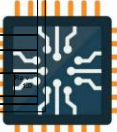
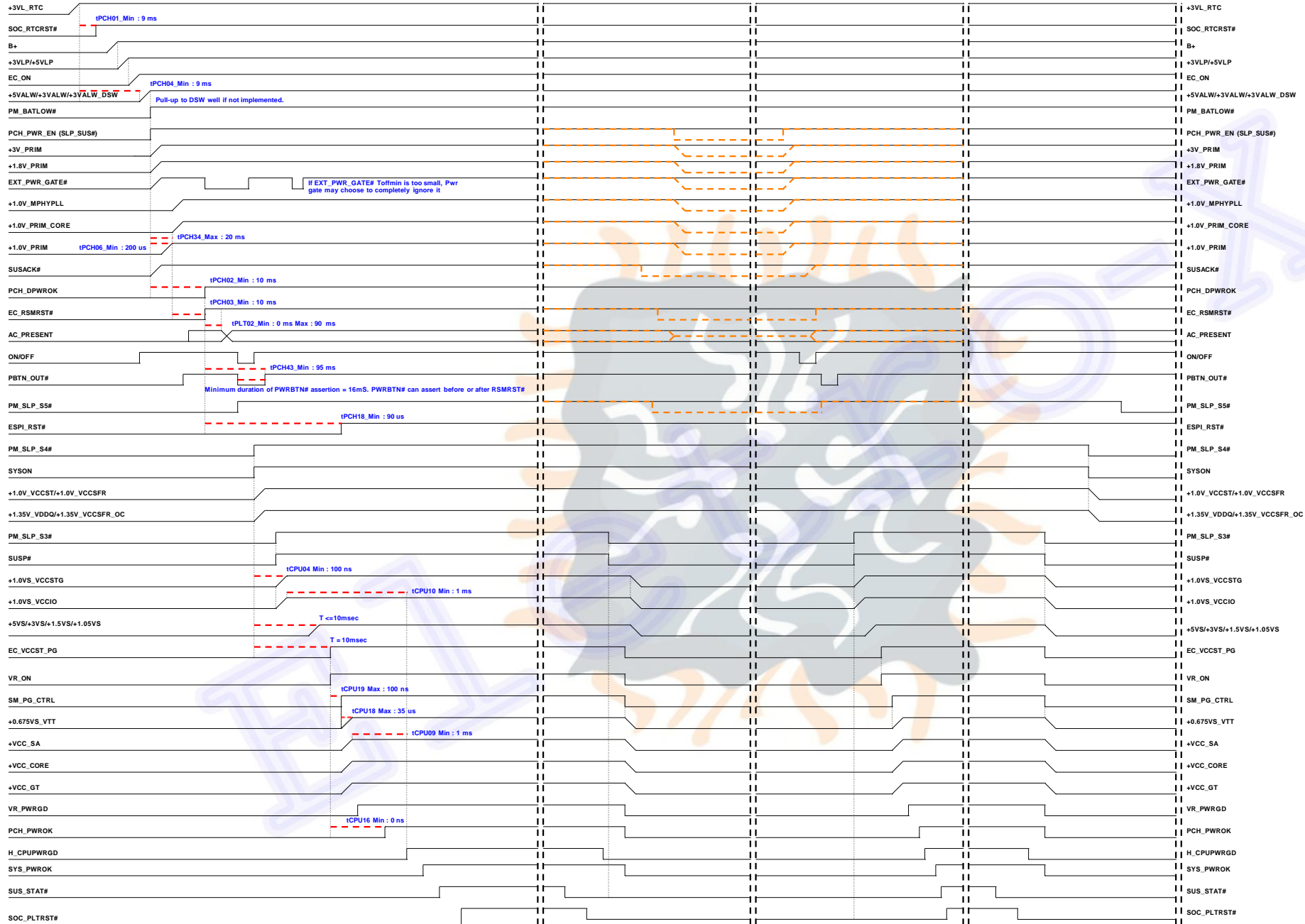


# G3->S0

# S0->S3/DS3

# S0/DS3->S0

# S0->S5





Voltage Rails

power plane	B+	+5VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE  +VCC GFXCORE_AXG +1.8VS +0.6VS +1.0VALW
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
I4" Only Components	I4@
I5" Only Components	I5@
HDMI Logo	45@
GIGA LAN Reserved Items	8111GLDO@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
GPU	N16S_R1@ N16S_R3@ N16V_R1@ N16V_R3@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
EMI Un-Mount Items	@EMI@
ESD Un-Mount Items	@ESD@
RF Un-Mount Items	@RF@
Connectors	ME@
Test Point	TP@
Intel Debug Components	@DCI@
Un-Mount Components	@
CPU Components - U22 Only	U22@
CPU Components - U42 Only	U42@
EMI U22 Components	U22_EMI@
EMI U42 Components	U42_EMI@
CPU	I3_7020U_R1@ I5_8250U_R1@ I5_8250U_R3@ I7_8550U_R1@ I7_8550U_R3@ I3_8130U_R1@

Item	BOM Structure
X4E	X4E_U22_I4@ X4E_U22_I5@ X4E_U42_I4@ X4E_U42_I5@
On Board RAM (Hynix 4GB)	H4G_MD@
On Board RAM (Micron 4GB)	M4G_MD@
On Board RAM (Samsung 4GB)	S4G_MD@
On Board RAM X76 Resistors	X76RAM@
Realtek Card Reader	RTK_CR@
Genesys Card Reader	GNS_CR@
VRAM (Hynix 2GB)	H2G_VRAM@ H2G@ H2G_R1@ H2G_R3@
VRAM (Hynix 4GB)	H4G_VRAM@ H4G@ H4G_R1@ H4G_R3@
VRAM (Micron 2GB)	M2G_VRAM@ M2G@ M2G_R1@ M2G_R3@
VRAM (Micron 4GB)	M4G_VRAM@ M4G@ M4G_R1@ M4G_R3@
VRAM (Samsung 2GB)	S2G_VRAM@ S2G@ S2G_R1@ S2G_R3@
VRAM (Samsung 4GB)	S4G_VRAM@ S4G@ S4G_R1@ S4G_R3@

USB 2.0 Port Table

Port	External USB Port
1	
2	USB2/3 Port (MB-1)
3	USB2/3 Port (MB-2)
4	
5	Camera
6	Card Reader
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	
2	USB2/3 Port (MB-1)
3	USB2/3 Port (MB-2)
4	
5	
6	

PCIe Port Table

Lane	Port	
1		
2		
3	1	GPU
4		
5		
6		LAN
7		NGFF WLAN+BT
8		
9		
10		
11		
12		

SATA Port Table

Port	
0	HDD
1	ODD

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x 16h	NCT7718W	1001 100x 98h

PCH SM Bus address GPU SM Bus address

Device	Address	Device	Address
DDR_0DIMM1	1010 000x A0h	Internal thermal sensor	1001 111x 9Eh
Touch Pad			

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1	NECP388	X	V	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW	+19 V_VN									
SMB_EC_CK2	NECP388	X	X	X	V	X	V	X	X	X	V	X	X
SMB_EC_DA2	+3VS		+3VGS										
SMB_EC_CK4	NECP388	X	X	X	X	X	X	X	X	X	X	V	X
SMB_EC_DA4	+3VALW												
PCH_SMBCLK	PCH	X	X	X	X	V	X	X	X	X	V	X	X
PCH_SMBDATA	+3VALW												
SML0CLK	PCH	X	X	X	X	X	X	X	X	V	X	X	X
SML0DATA	+3VALW												
SML1CLK	PCH	X	X	X	V	X	X	X	X	X	X	X	X
SML1DATA	+3VALW												

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

GPU

U1# N16S_R1@	U1# N16V_R1@
N16S-GTR-S-A2 BGA 595P SA0000B1H10	N16V-GMR1-S-A2 BGA 595P SA0000B1H10
U1# N16S_R3@	U1# N16V_R3@
N16S-GTR-S-A2 BGA 595P SA0000B1H10	N16V-GMR1-S-A2 BGA 595P SA0000B1H10

CPU

U1# I3_7020U_R1@
QNZU1702.3G SA0000B1H10
U1# I3_7020U_U22@
SR3TR1702.3G SA0000B1H10

X4E

U42 X4E_U42@ X4E_U42@ X4E_U42@ X4E_U42@	U22 X4E_U22@ X4E_U22@ X4E_U22@ X4E_U22@
---	---

GD5R5 VRAM \* 2

2GB
H2G_VRAM@ H2G@ H2G_R1@ H2G_R3@
X76 HYNIX 2GB X76 MICRON 2GB X76 SAMSUNG 2GB

ON BOARD RAM \* 4

S4G_MD@ M4G_MD@ H4G_MD@
X76 SAMSUNG 4GB MD X76 MICRON 4GB MD X76 HYNIX 4GB MD

CARD READER

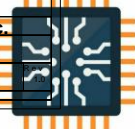
\*Main Source - Realtek  
\*Substitute - Genesys

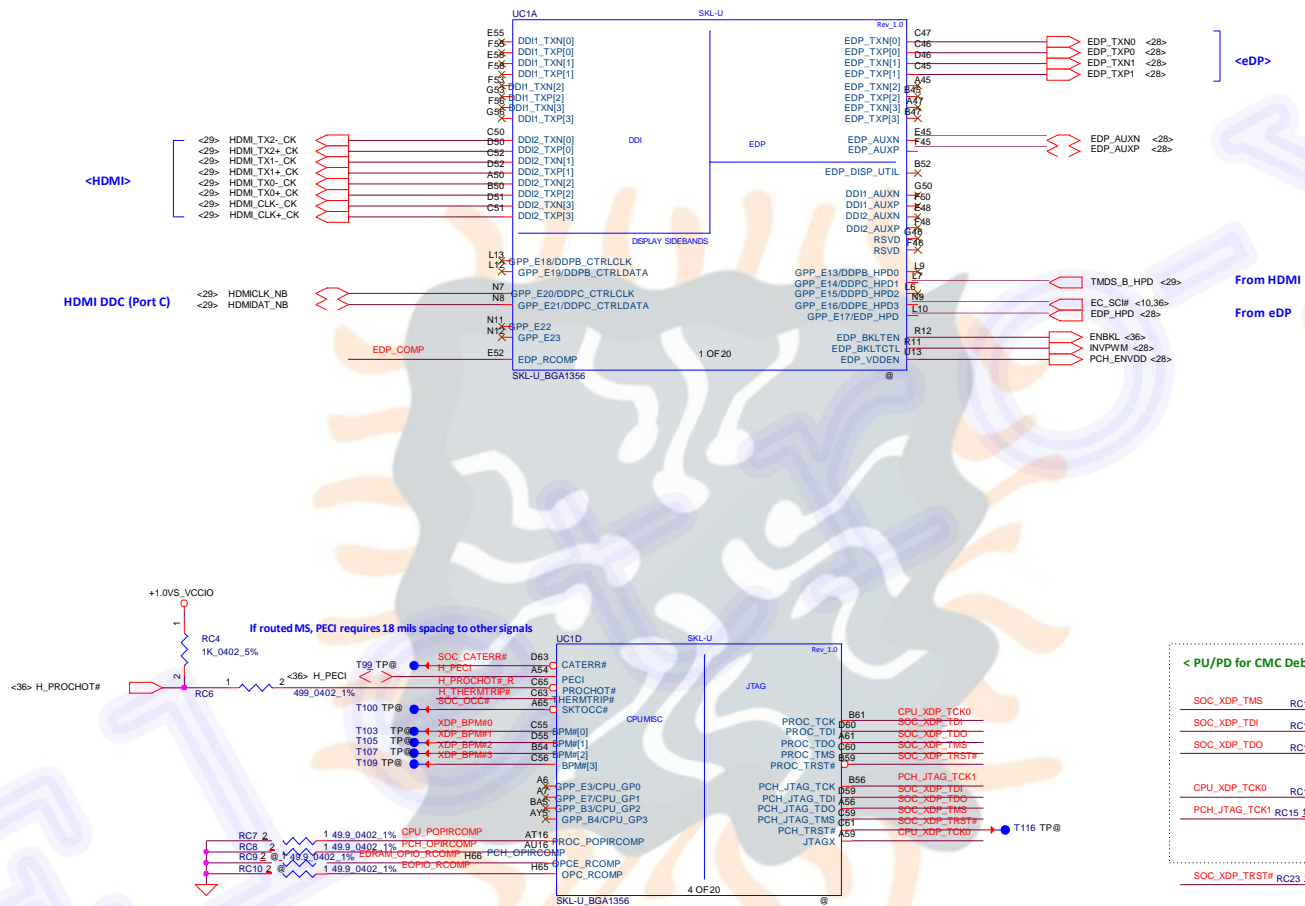
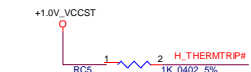
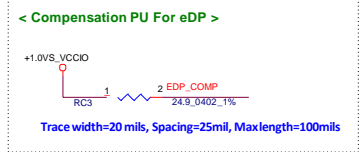
HDMI Logo

45@
HDMI Logo RO0000003HM

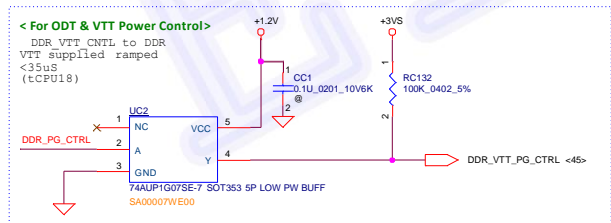
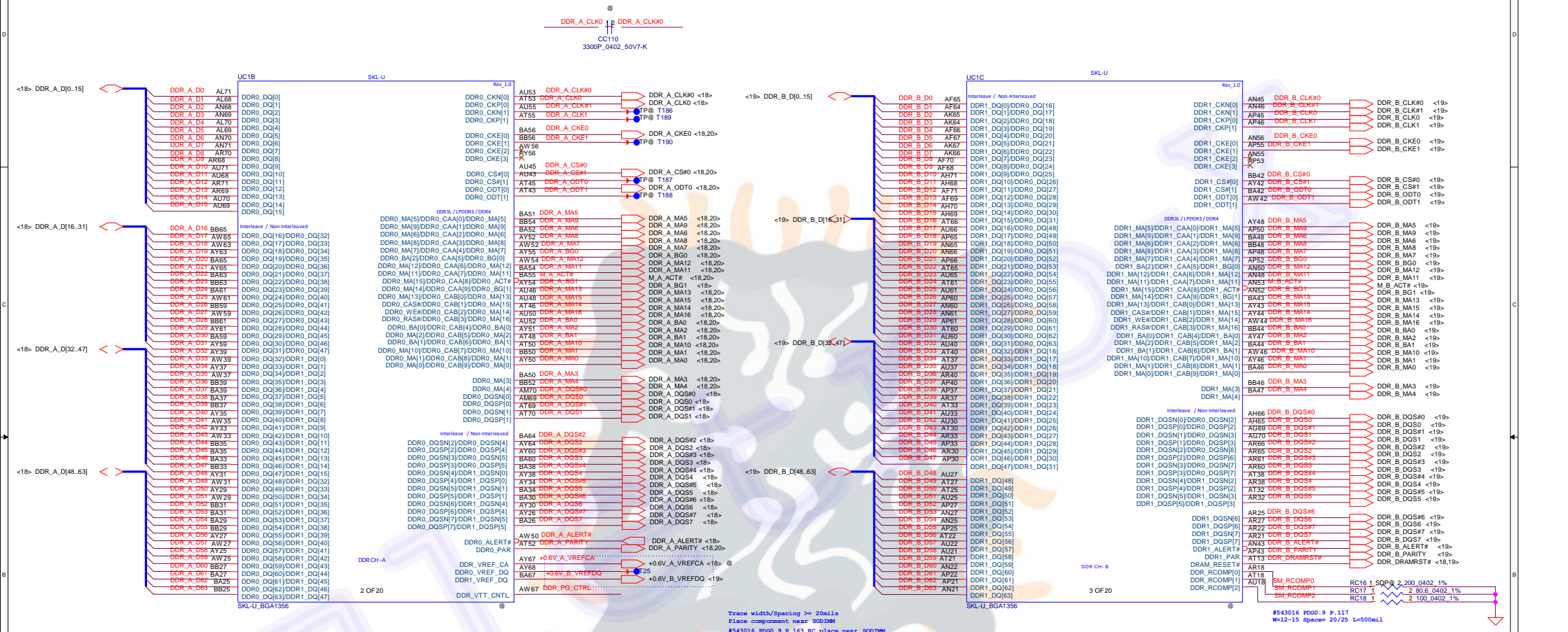
PCB

DA22A000201
DA22A000201

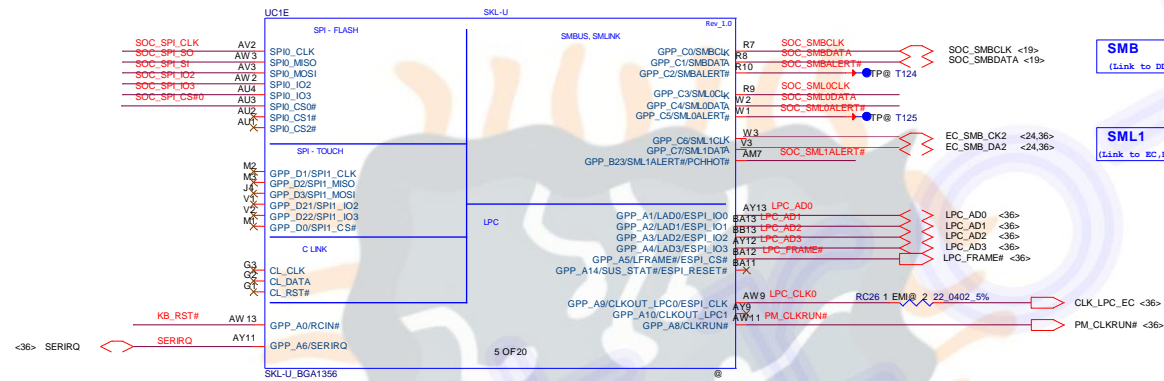
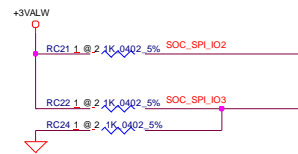




# Interleaved Memory





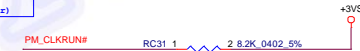
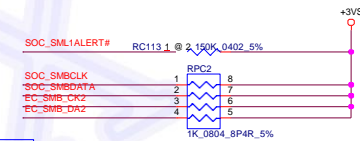
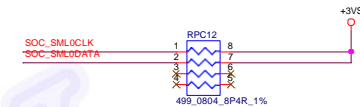


SML0ALERT# (Internal Pull Down):

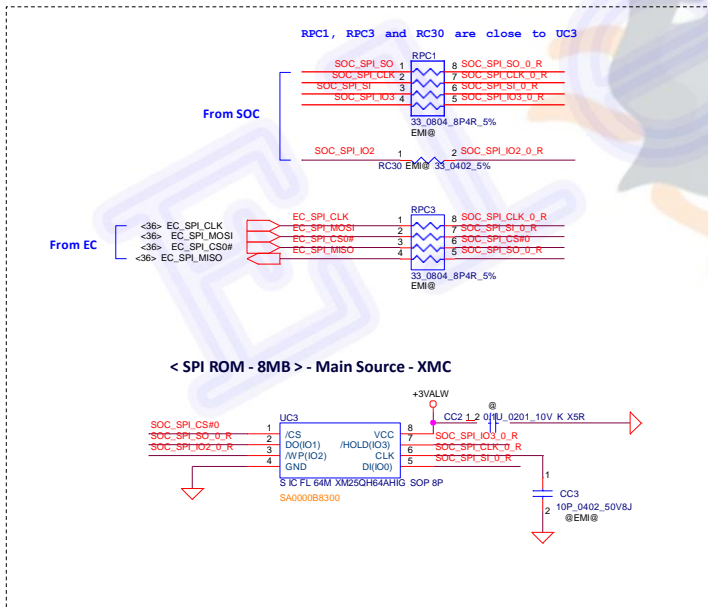
eSPI or LPC

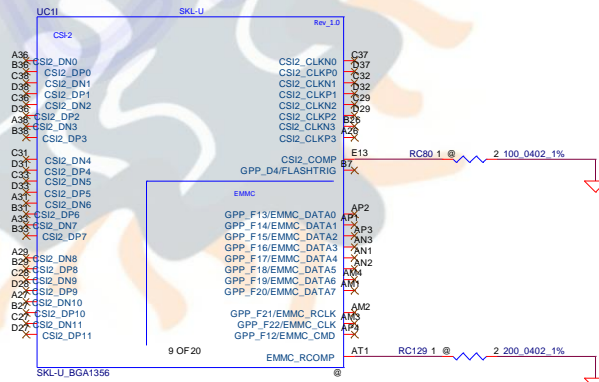
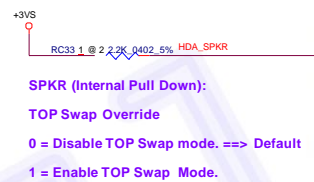
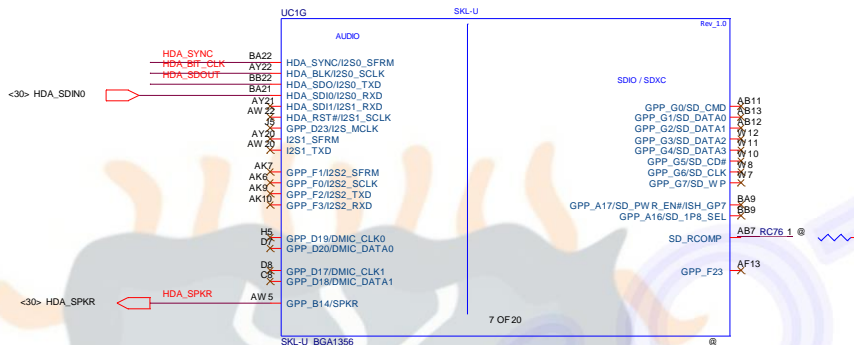
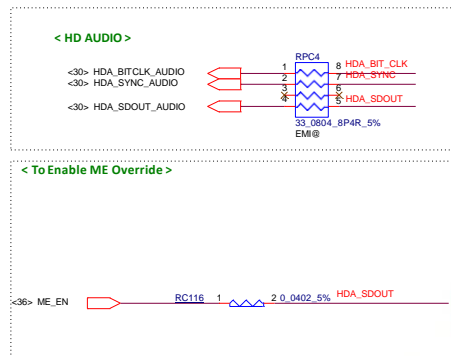
0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

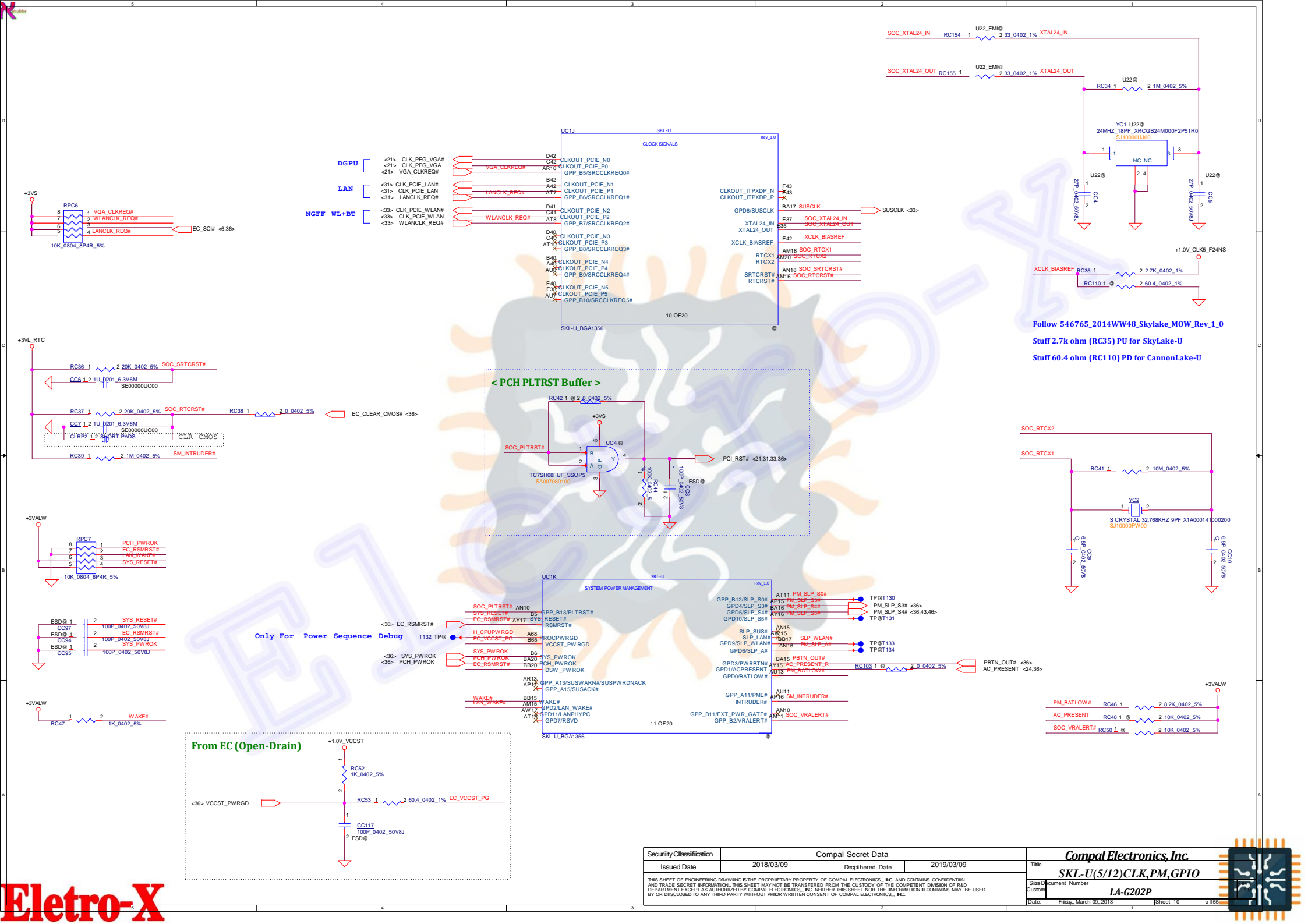


Follow 543016\_SKL\_U\_Y\_PDG\_0\_9









GSPI0\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

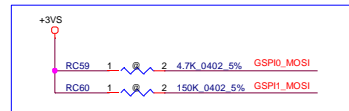
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1\_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

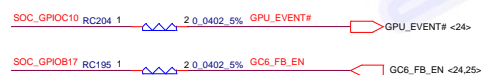
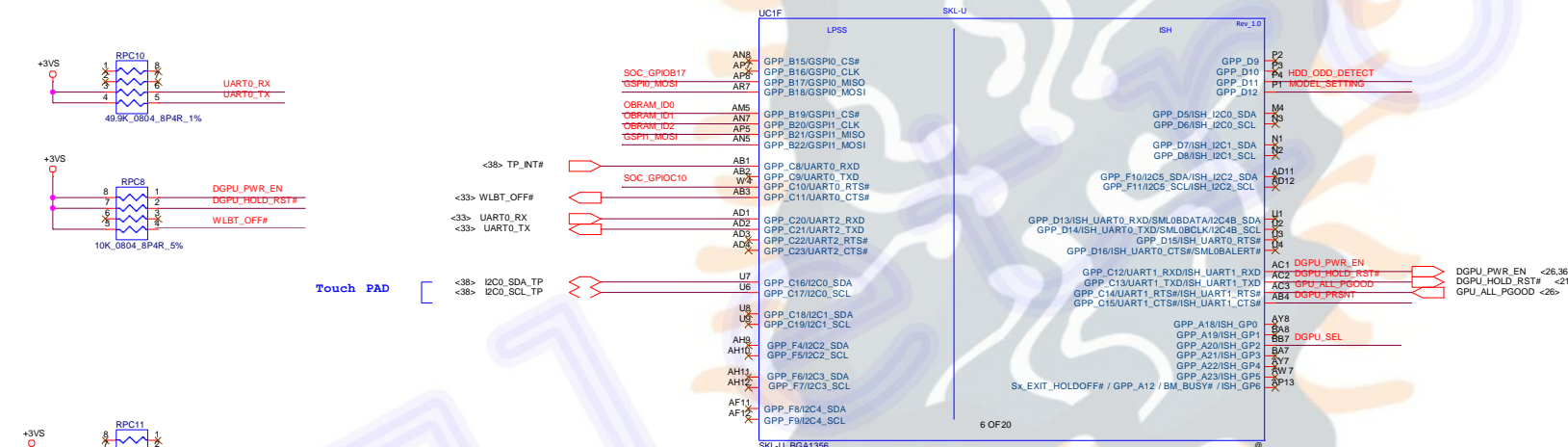
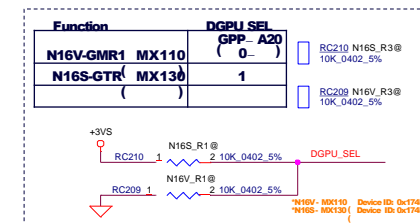
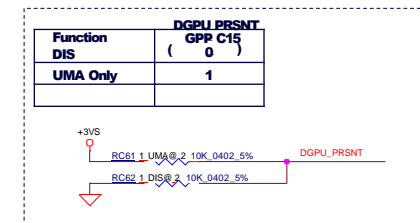
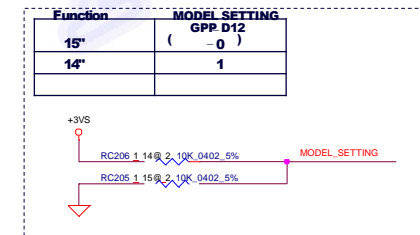
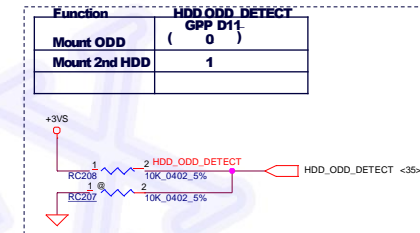
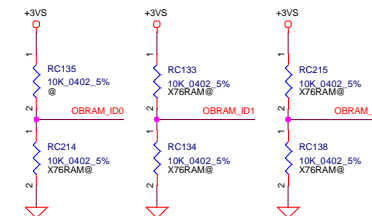
0 = SPI Mode ==> Default

1 = LPC Mode

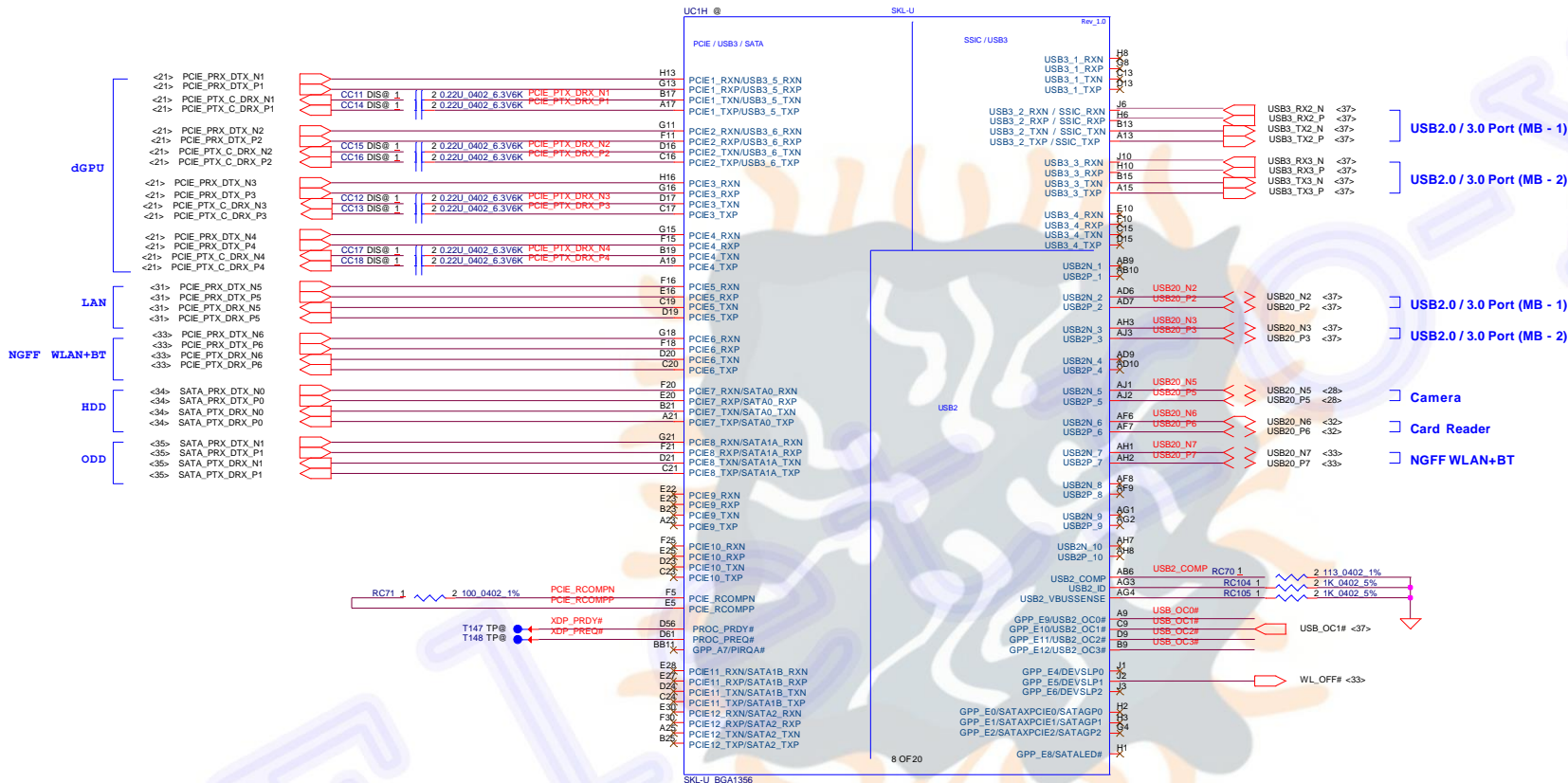


Capacity	Description	X76	PART NUMBER R3
4GB	WITHOUT ON-BOARD RAM	N/A	N/A
	SAMSUNG 2666MHz K4A8G165WC-BCTD	X7677538L13	SA0000B6F10
	HYNIX 2666MHz H5A8N8G6NCJR-VKC	X7677538L15	SA0000BMN10
	MICRON 2666MHz MT40A512M16LY-075E	X7677538L14	SA0000ARD30
	N/A	N/A	N/A
	N/A	N/A	N/A
	N/A	N/A	N/A

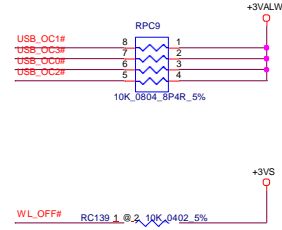
Capacity	Description	GPP B19 OBRAM ID	GPP B20 OBRAM ID	GPP B21 OBRAM ID
4GB	WITHOUT ON-BOARD RAM	0 -	0 -	0 -
	SAMSUNG 2666MHz K4A8G165WC-BCTD	0	0	1
	HYNIX 2666MHz H5A8N8G6NCJR-VKC	0	1	0
	MICRON 2666MHz MT40A512M16LY-075E	0	1	1
	N/A	1	0	0
	N/A	1	0	1
	N/A	1	1	0



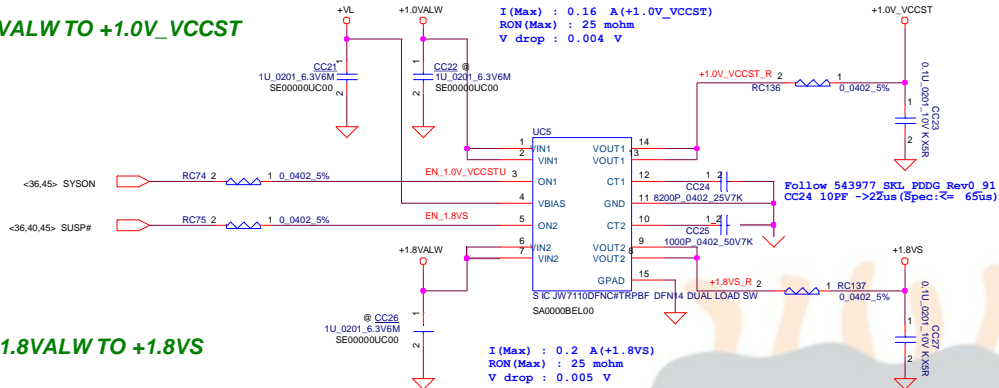
TO DGPU



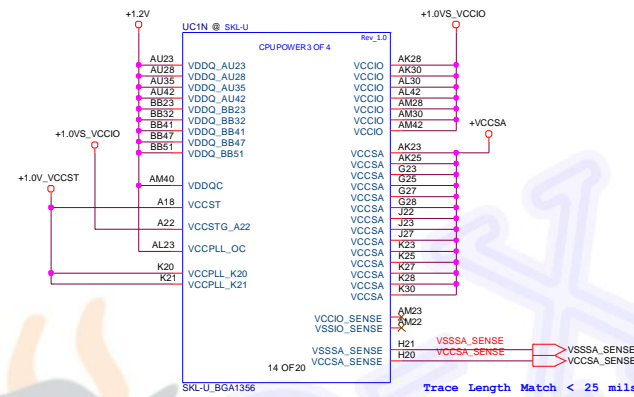
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.



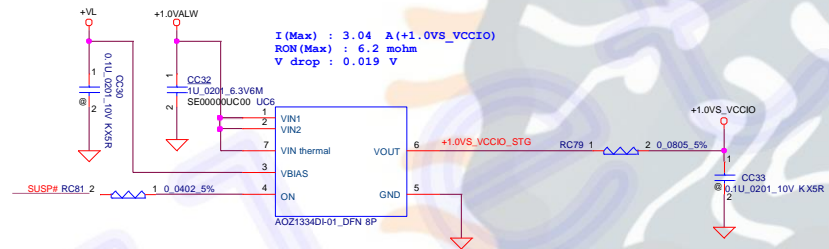
**+1.0VALW TO +1.0V\_VCCST**



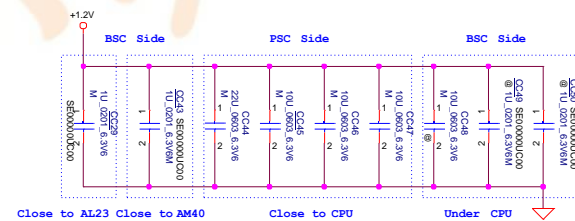
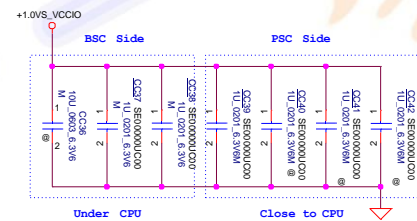
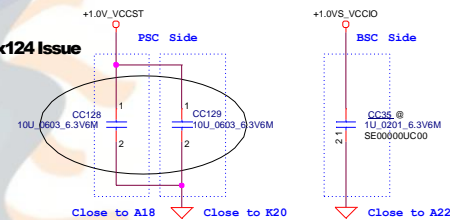
**+1.8VALW TO +1.8VS**



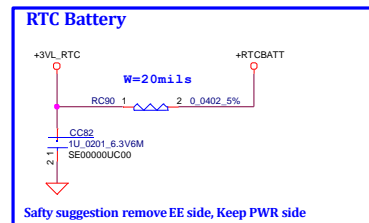
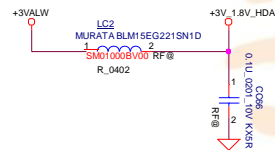
**+1.0VALW TO +1.0VS\_VCCIO**



**Reserved for BSoD 0x124 Issue**

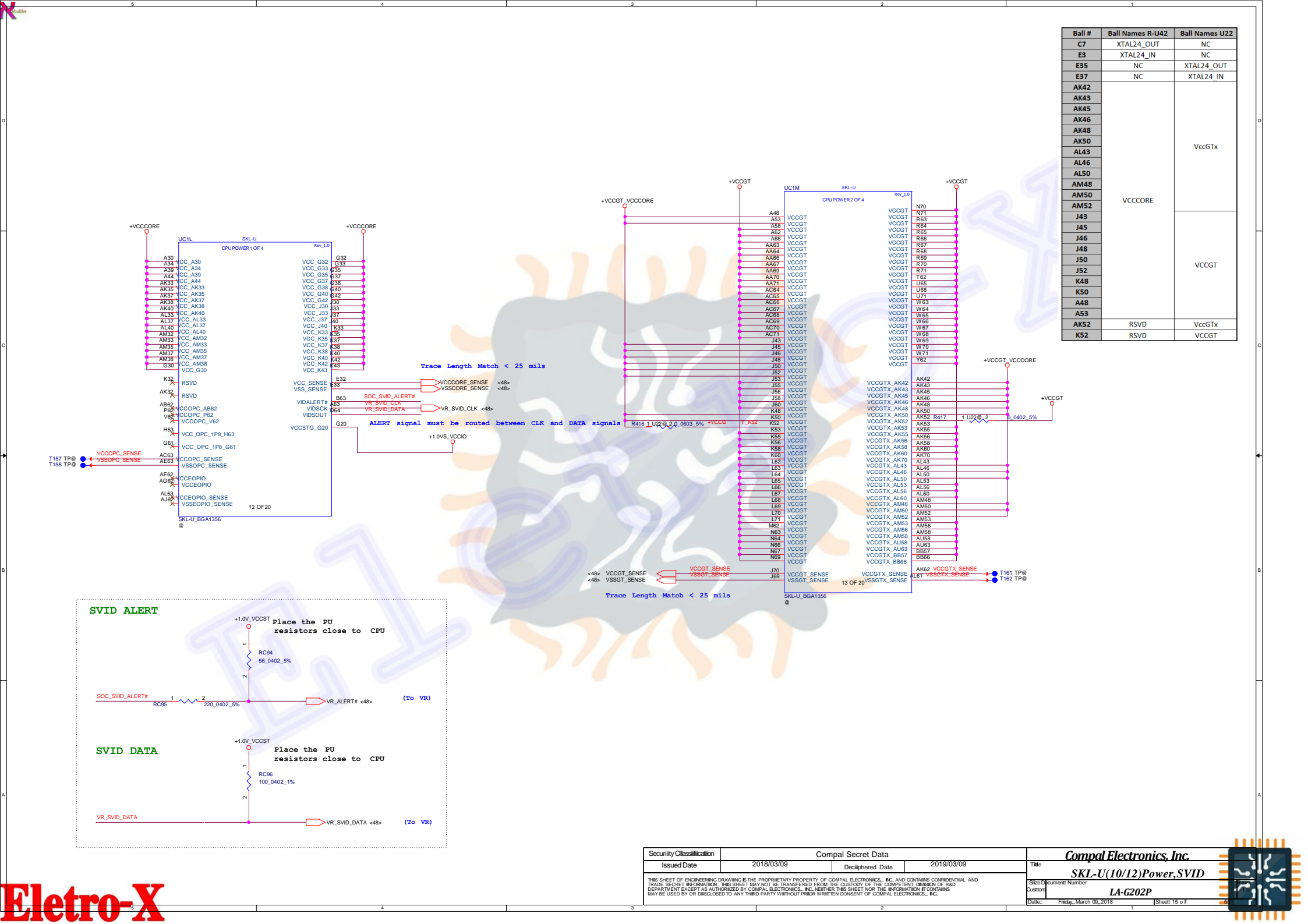






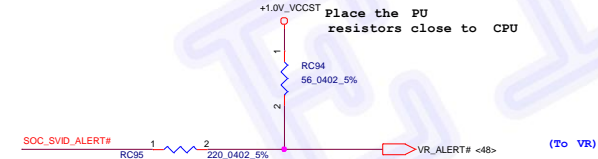
# Eletro-X



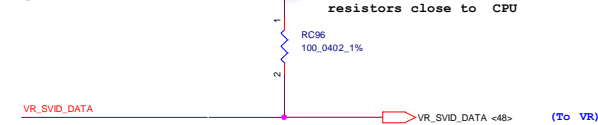


Ball #	Ball Names R-U42	Ball Names U22
C7	XTAL24_OUT	NC
E3	XTAL24_IN	NC
E35	NC	XTAL24_OUT
E37	NC	XTAL24_IN
AK42		
AK43		
AK45		
AK46		
AK48		
AK50		
AL43		
AL46		
AL50		
AM48		
AM50		
AM52		
J43		
J45		
J46		
J48		
J50		
J52		
K48		
K50		
A48		
A53		
AK52	RSVD	VccGTx
K52	RSVD	VCCGT

# SVID ALERT



# SVID DATA



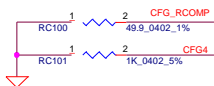
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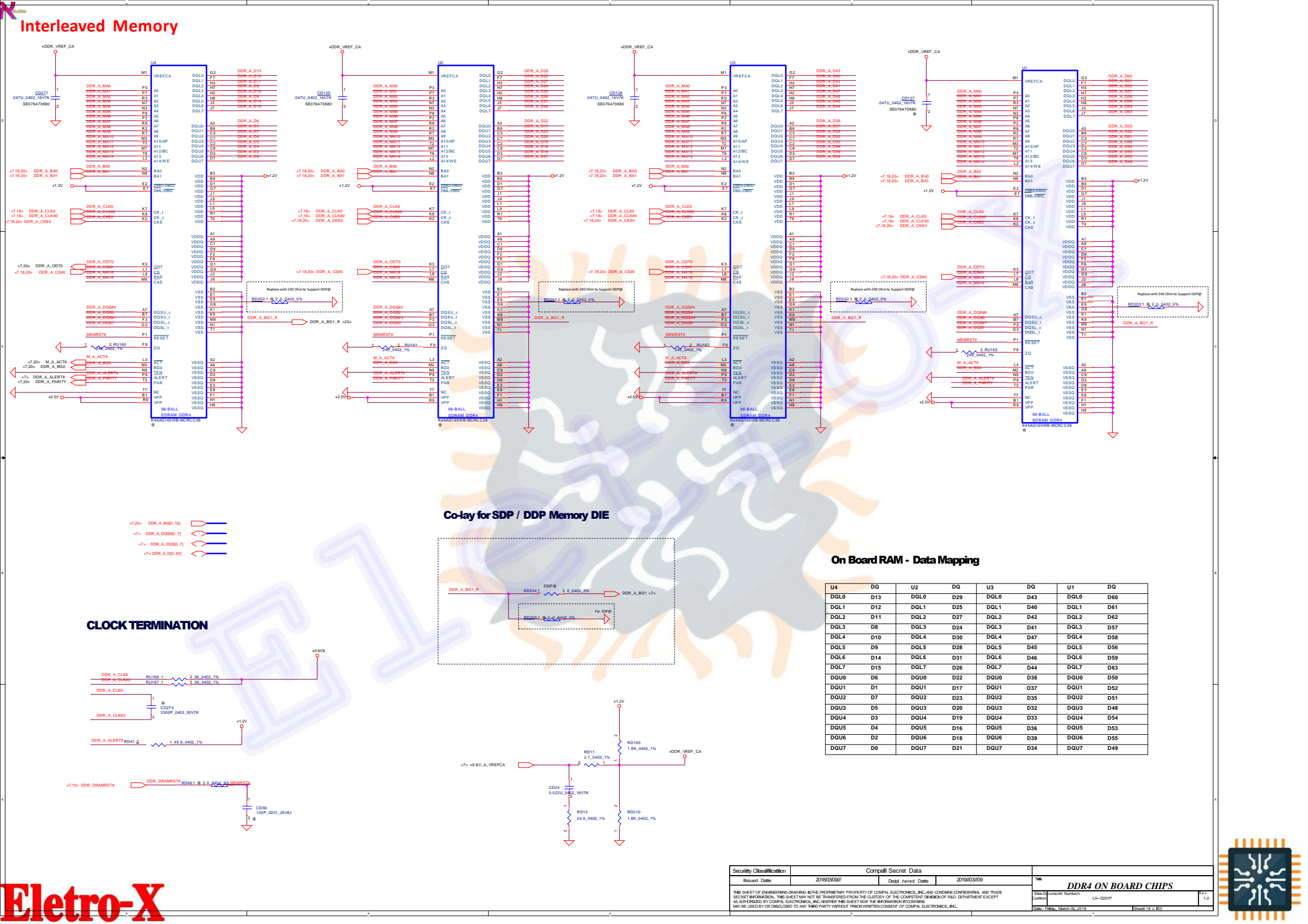
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Document Number		SKL-U(11/12)GND
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DDR\_A\_B01\_R

DDPB

RD2551

$20k\Omega$

$C2551$

$0.047\mu F$

DDR\_A\_B01<7>

RD2552

$20k\Omega$

$C2552$

$0.047\mu F$

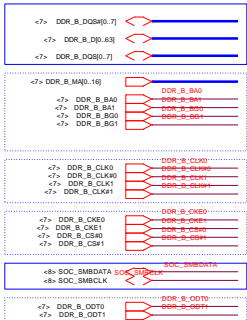
For SDRB

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

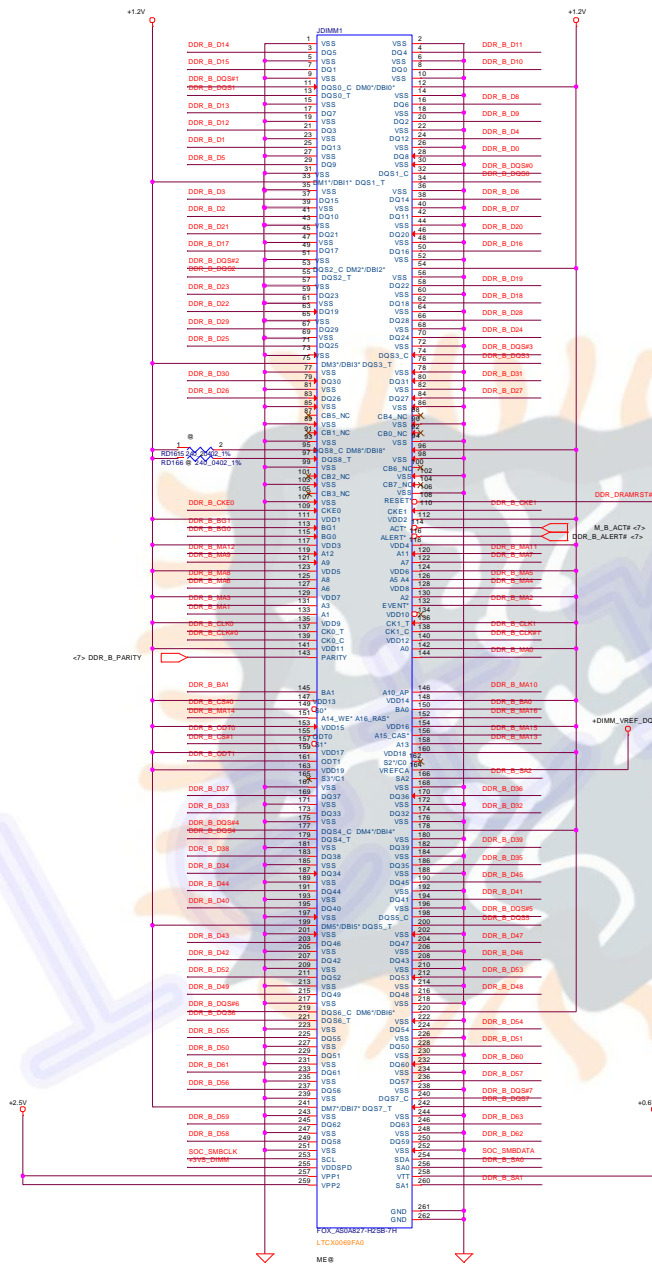
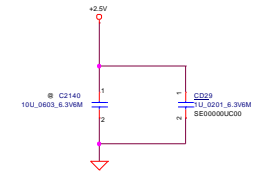
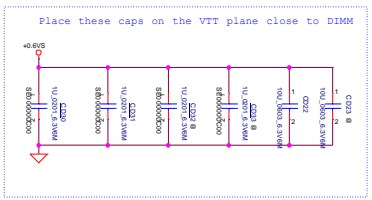
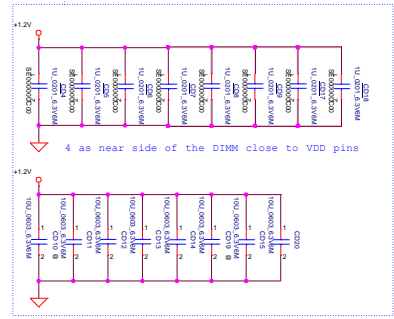
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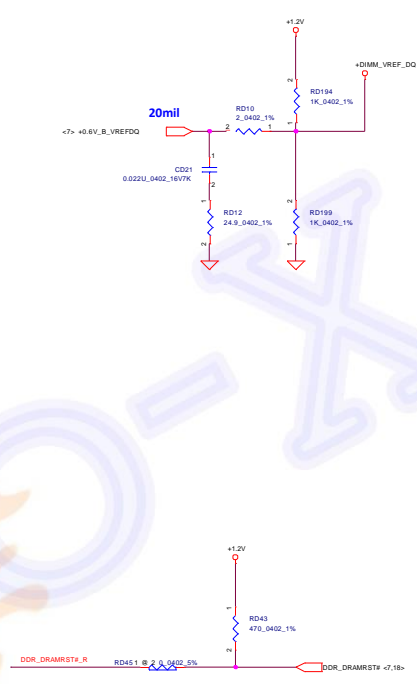


**Layout Note:**  
Place near JDIMM1

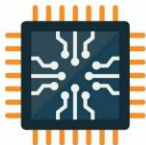
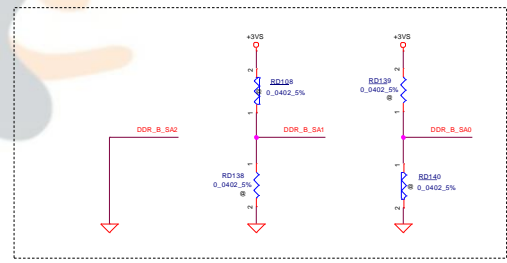
**Note:**  
Check voltage tolerance of VREF\_DQ at the DIMM socket



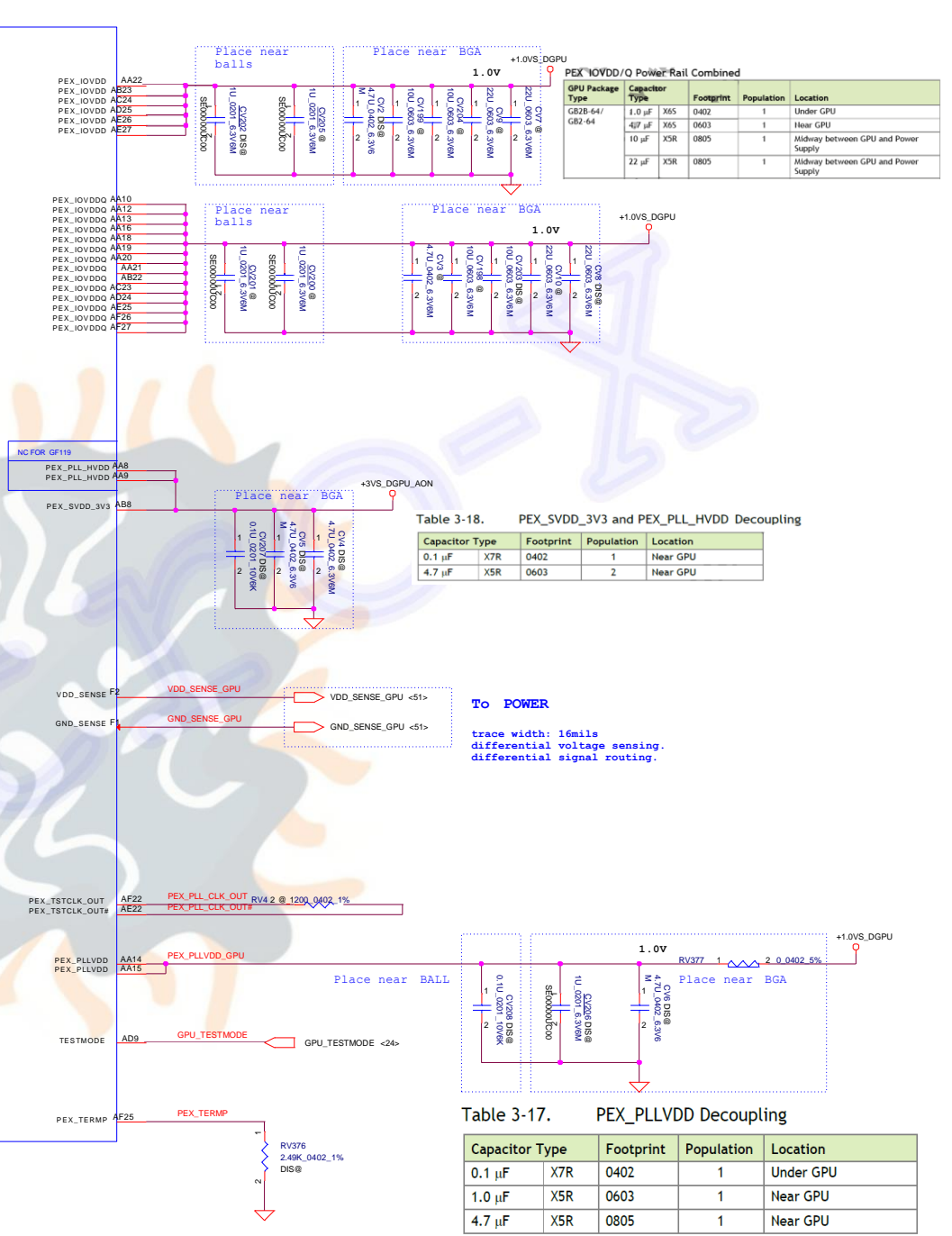
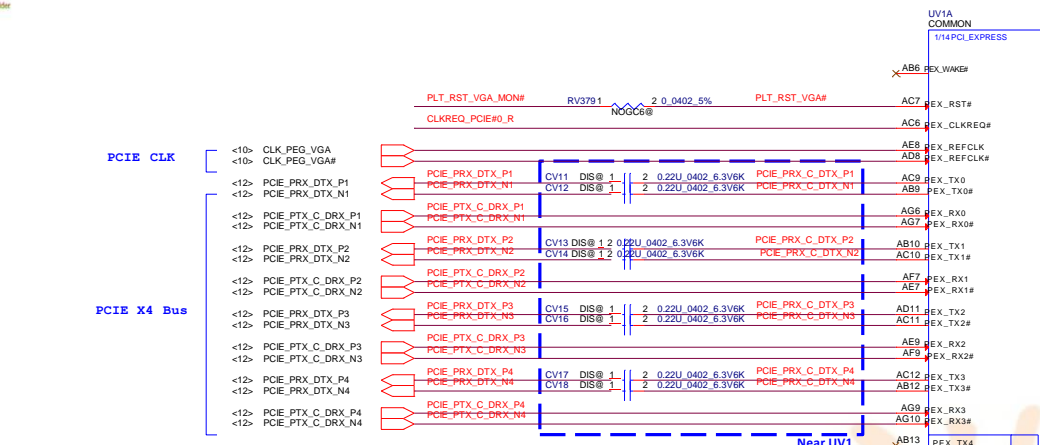
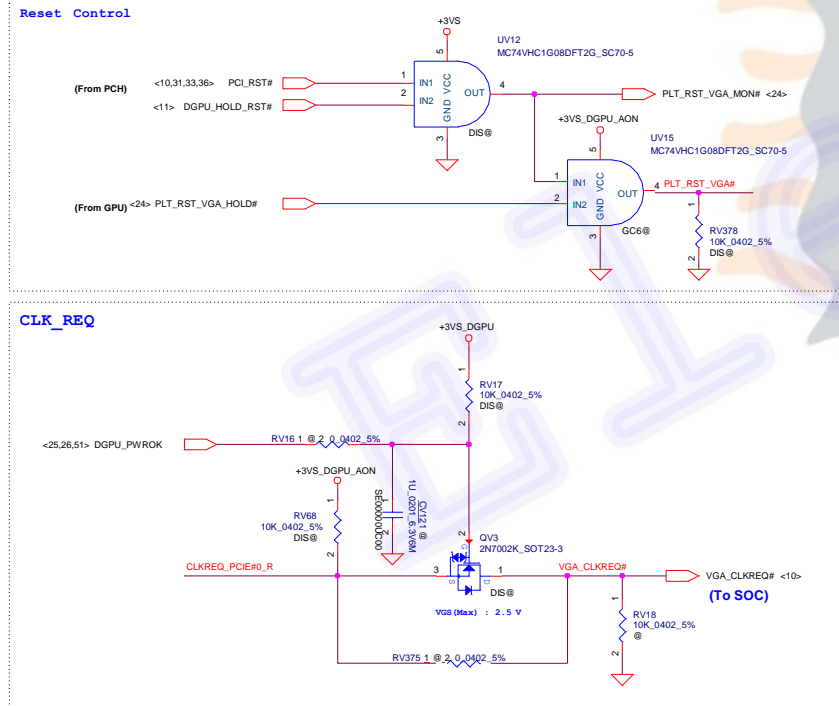
**Reverse Type**  
2-3A to 1 DIMMs/channel



**JDIMM1 ADDRESS PLACE CLOSE TO DIMM**

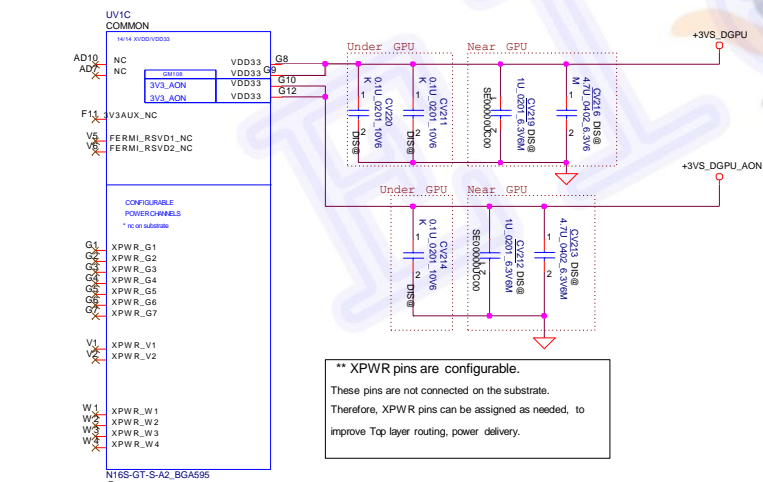








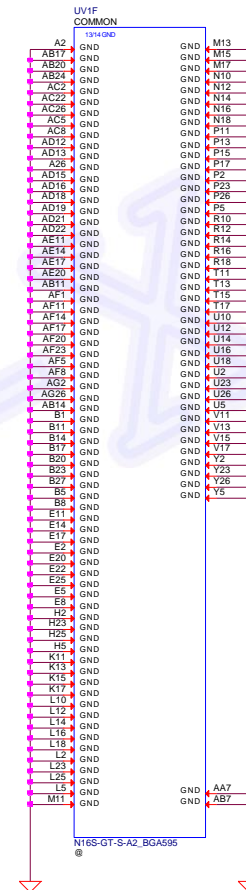
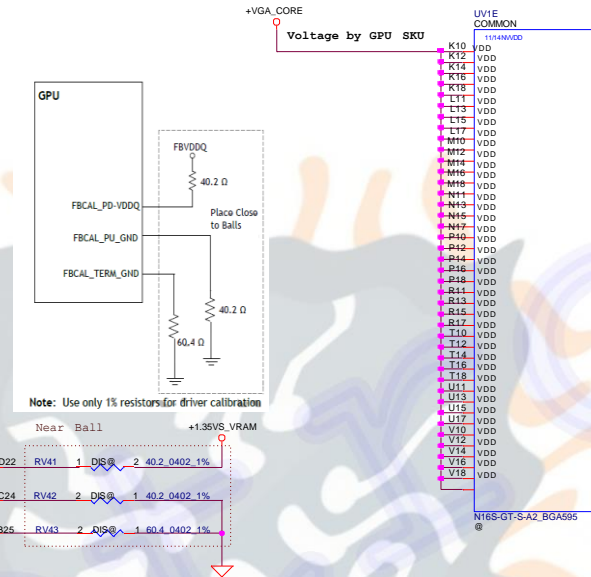
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64/	0.1 $\mu$ F	X7R 0402	2	Under GPU
GB2-64	1 $\mu$ F	X7R 0603	2	Under GPU
GDDR5	4.7 $\mu$ F	X6S 0603	2	Under GPU
	10 $\mu$ F	X5R 0805	1	Near GPU
	22 $\mu$ F	X5R 0805	1	Near GPU



GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2-64	3V3_MAIN	0.1 $\mu$ F	X6S 0402	2	Under GPU
GB2B-64		1 $\mu$ F	X5R 0603	1	Near GPU
GB4B-128		4.7 $\mu$ F	X5R 0603	1	Near GPU
GB3B-256					
GB2-64	3V3_AON	0.1 $\mu$ F	X6S 0402	1	Under GPU
GB2B-64		1 $\mu$ F	X5R 0603	1	Near GPU
GB4B-128		4.7 $\mu$ F	X5R 0603	1	Near GPU
GB3B-256					

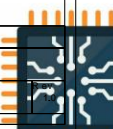
Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

## GPU Decoupling CAPs @ Power Page

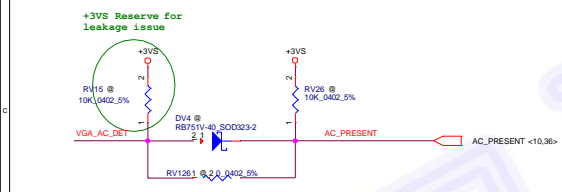
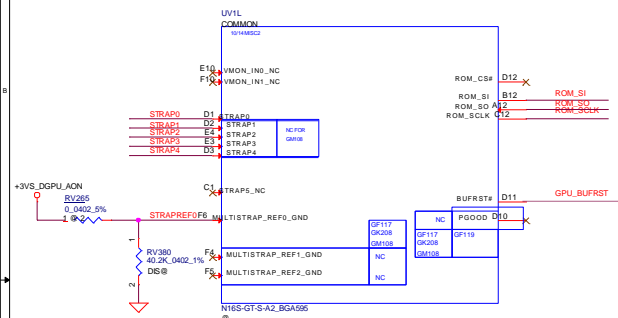
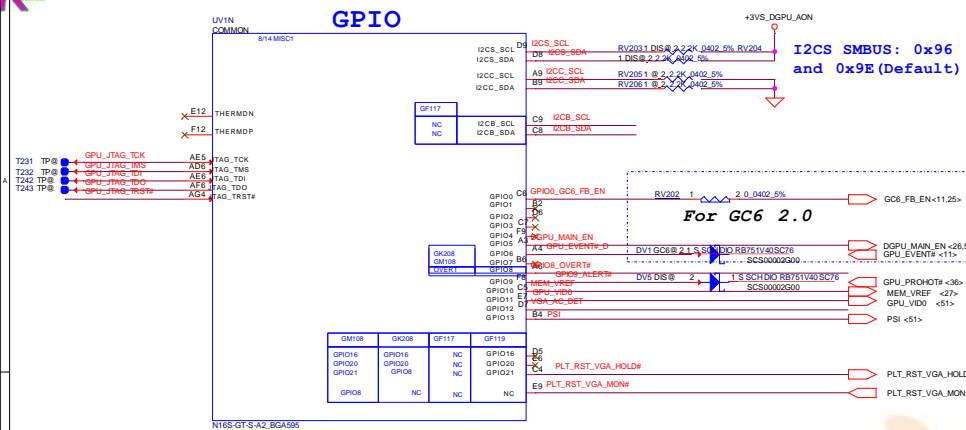


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RAM_CFG	X76	CONFIG	ROM_SI
0x0 4.99K (L)	X7677538L04	S2G@	RV55 4.99K+1%0402 SD03489910 S2G@
0x1 10.0K (L)	X7677538L05	M2G@	RV55 10K+1%0402 SD03410020 M2G@
0x5 30.1K (L)	X7677538L06	H2G@	RV55 30.1K+1%0402 SD03430120 H2G@
0x6 34.8K (L)			RV55 34.8K+1%0402 SD03448280 @
0x7 45.3K (L)			RV55 45.3K+1%0402 SD03445320 @
0x4 24.9K (L)			RV55 24.9K+1%0402 SD03448280 @

Table 13. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories							
Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver <sup>1</sup>
	Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver <sup>1</sup>
	Hynix	H5GCBH24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
	Hynix	H5GCBH24MJR-ROC	M-die	0x5	3000	N/A	Substitution allowed with waiver <sup>1</sup>
	Hynix	H5GQBH24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver <sup>1</sup>
	Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready
	Micron	MT51J256M32HF-70-A	A-die	0x1	3000	N/A	Substitution allowed with waiver <sup>1</sup>
	Micron	MT51J256M32HF-80-A	A-die	0x1	3000	N/A	Substitution allowed with waiver <sup>1</sup>

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEV_ID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9k pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

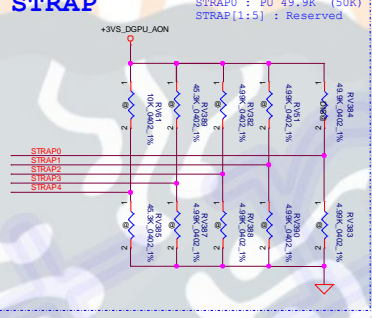
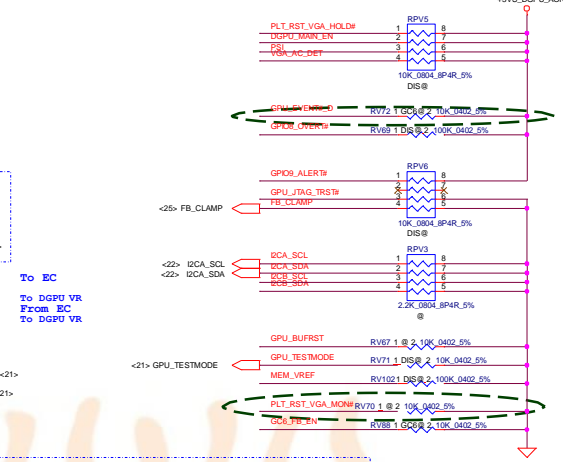
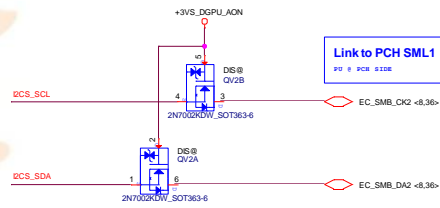


Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GCA_FB_EN	O	FB Enable for GCA 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GCA 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GCA 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3D_Vision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side flow-reset monitor	10 kΩ pull-up to 3V3_AON
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VDD	O	GPU Gate VDD PWM control signal	100 kΩ pull-up to 3V3_AON
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10k pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFA used as DisplayPort or for IFAA when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

Item	N16P-GT	N16S-GT-B/S
Device ID	0x139A	0x1347
Package	GB4B-128	GB4B-128/GB2B-64
Internal P/N	GM107-750,28nm	GM108-755/655,28nm
ROM_SI	Refer to N16X_RAM_Straps table	Refer to N16X_RAM_Straps table
ROM_SO	0x0000, 4.99Kohm pull down	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default)
Strap2		
Strap3		
Strap4		
Open_VRG SKU	B	B
NVDD Boot Voltage	0.9V	0.9V

### Internal Thermal Sensor



RAM\_CFG[3:0] BAX40 (ROM\_S1)

0x0	4.99K (L)	\$2G@
0x1	10.0K (L)	\$2G@
0x2	15.0K (L)	
0x3	20.0K (L)	
0x4	24.9K (L)	
0x5	30.1K (L)	\$2G@
0x6	34.8K (L)	
0x7	45.3K (L)	
0x8	4.99K (H)	
0x9	10.0K (H)	
0xA	15.0K (H)	
0xB	20.0K (H)	
0xC	24.9K (H)	
0xD	30.1K (H)	
0xE	34.8K (H)	
0xF	45.3K (H)	

### 10.2.1 Unconnected Signals (NC)

Do not route unused PC signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

### 10.2.2 I<sup>2</sup>C Slave Address

N16X GPUs use the FCS slave address 0x96h for NVIDIA internal testing. PC address 0x96h must not be used by other PC devices on the same bus as the GPU to avoid address conflict. The SMB\_ALT\_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful PCS SML addresses can be used with SMB\_ALT\_ADDR strap.

### 16.3.3 Internal Thermal Sensor Interface

The internal thermal sensor can be accessed through the FCS interface as described in the PC chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the FCS interface by the system is not supported. The default port address to access the internal thermal sensor over the FCS is 0x9E. Table 16-1 describes the byte-wise registers accessible through the FCS interface.





[illegible]

**+3VS to +3VS\_DGPU\_AON**

The schematic diagram illustrates the power switcher circuit for the +3VS to +3VS\_DGPU\_AON. The circuit is powered by a +5VSW source and a +3VS source. The output is +3VS\_DGPU\_AON. A signal <11.36> DGPU\_PWR\_EN is connected to the circuit.

Key components and their values:

- Resistors: RV258 (47K, 0.402, 5% DIS), RV264 (0.402, 5%), RV259 (10K, 0.402, 5%), RV261 (4.7K, 0.402, 5%).
- Transistors: QV20 (DIS), QV30B (DIS), QV19 (2N7002), QV21 (2N7002).
- Diodes: CQ117 (1.5V, 0.010, 5%), CQ115 (1.5V, 0.010, 5%).

The circuit includes a +5VSW input, a +3VS input, and a +3VS\_DGPU\_AON output. A signal <11.36> DGPU\_PWR\_EN is connected to the circuit.

Schematic diagram of the DGPU\_PWRON signal path. The signal originates from a source labeled <21.25.51> DGPU\_PWRON, passes through a buffer (D4), and then through a series of inverters (SC30002G00, SC30002G00, DISB) to a node labeled GPU\_ALL\_PGOOD. This node is also connected to a pull-up resistor R382 (10K, 0402, 5%) to a +3V3\_DGPU\_AON supply. A second signal path, labeled <52> +1.35VGS\_PGOOD, passes through a resistor R383 (2.0, 0402, 5%) to the same GPU\_ALL\_PGOOD node. The final output is labeled GPU\_ALL\_PGOOD <11>.



Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

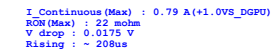
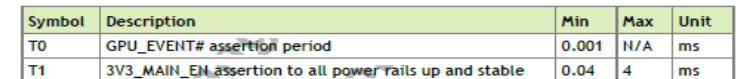


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram



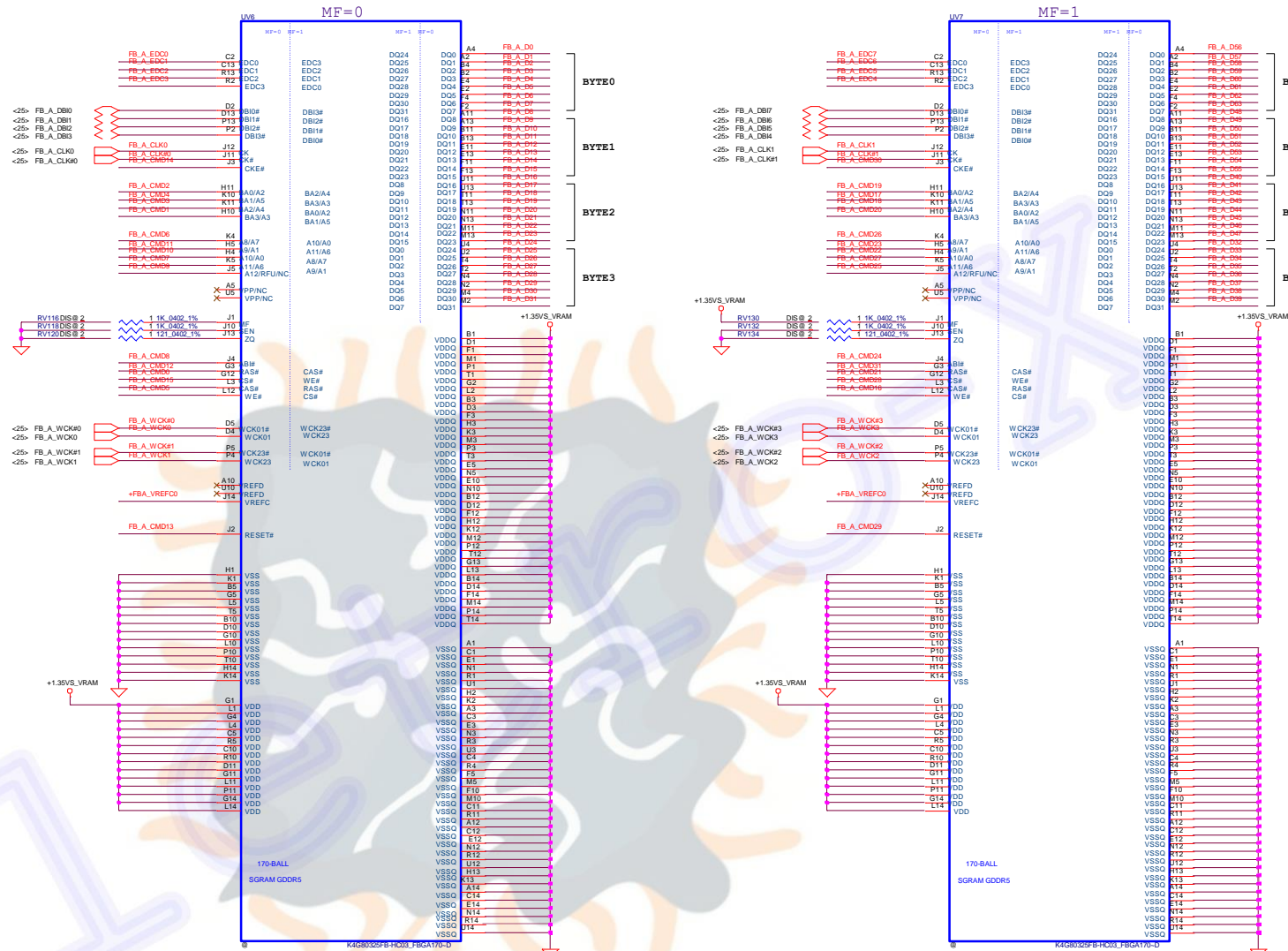
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During G6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in G6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

# VRAM Memory Partition A

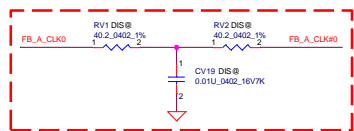
Table 7-4. GDDR5 Mode H Mapping

G82-64, G82B-64, G84B-128	Channel 0 0..31	G82-64, G82B-64, G84B-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CA5*	CMD31	CA5*
CMD32	Hot_unused		
CMD33	Hot_unused		
CMD34	DEBUG2		
CMD35	DEBUG1		

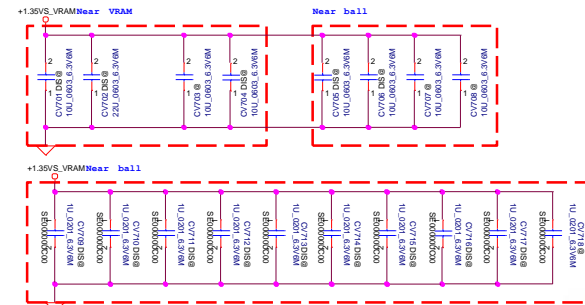
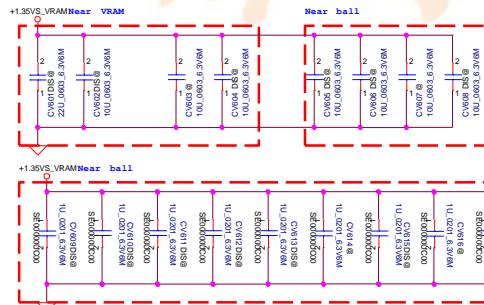
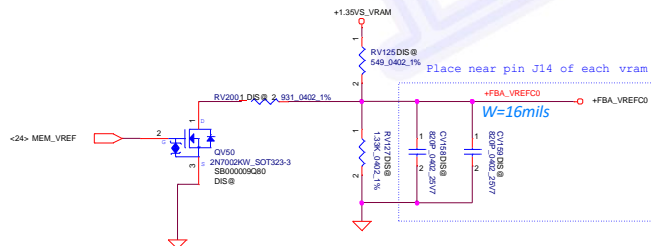
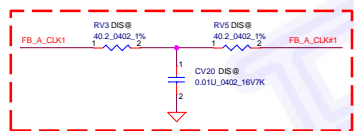
Notes:  
 1. Not available in G82-64 and G82B-64 packages.  
 2. GPU debug pins not connected to URAM. See section 7.1.13.



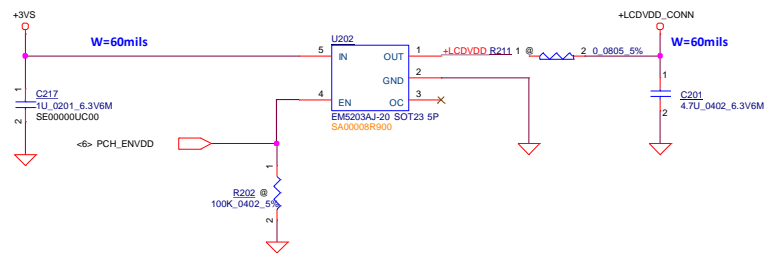
Near to UV6



Near to UV7



## LCD POWER SWITCH



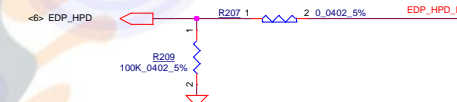
## CAMERA POWER CIRCUIT



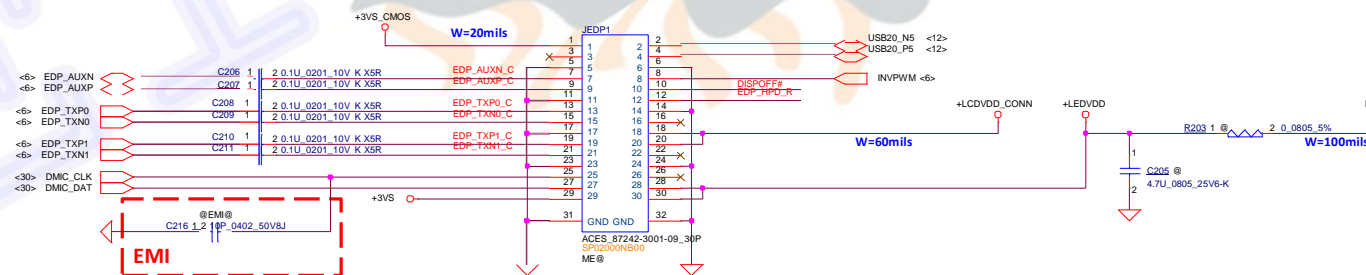
## DISPLAY OFF



## HOT PLUG DETECT

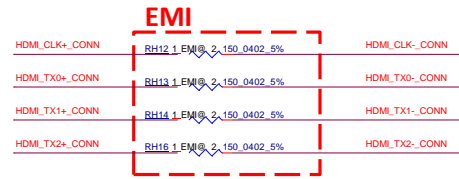
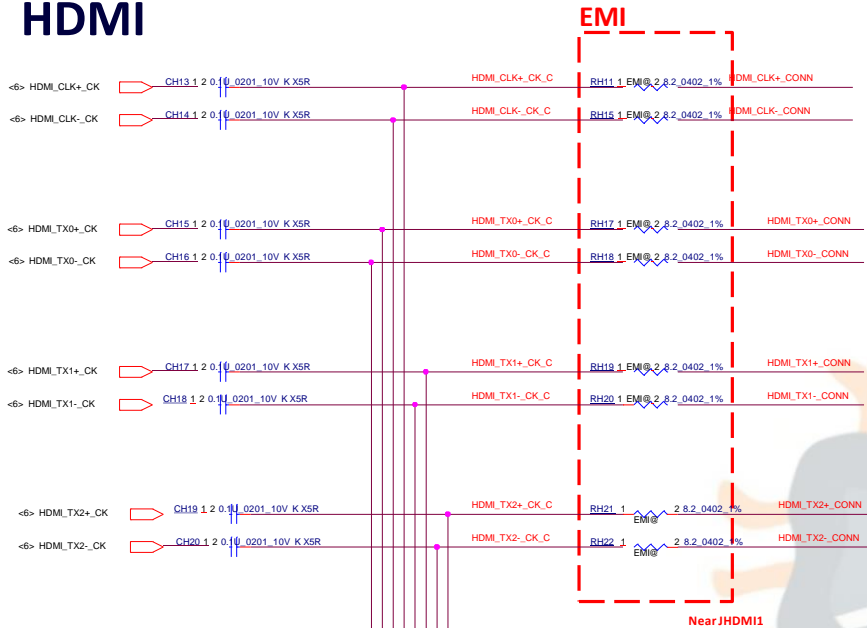


## eDP CONNECTOR

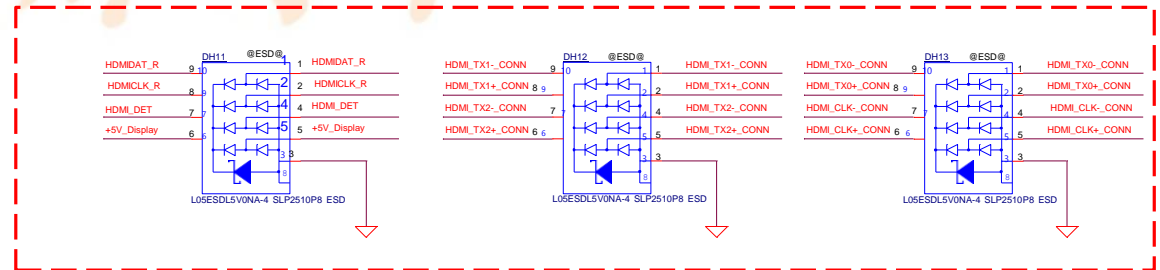
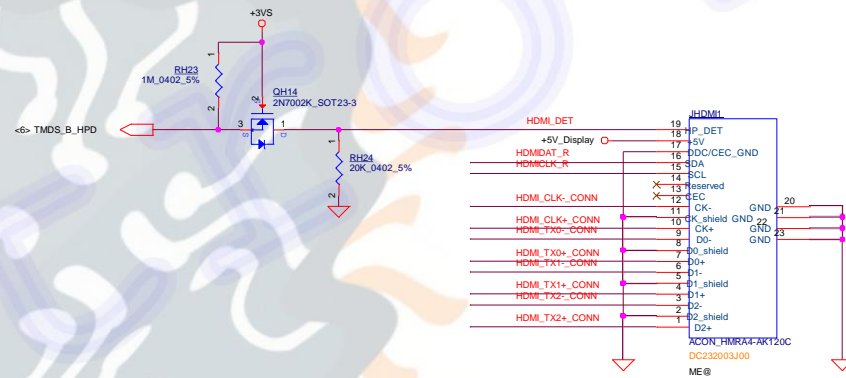
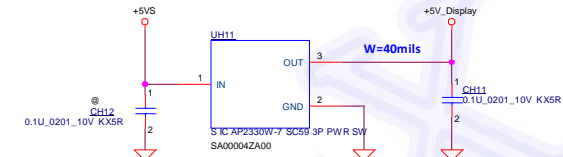


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# HDMI



For HDMI

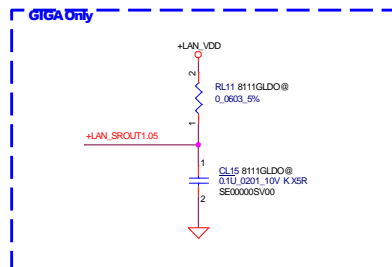
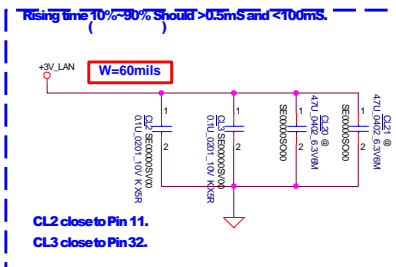
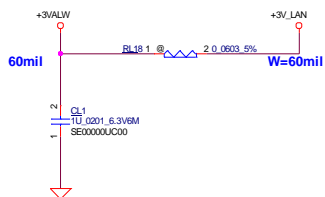


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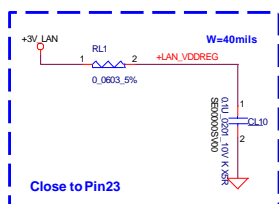
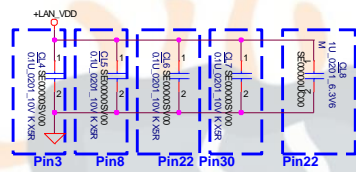
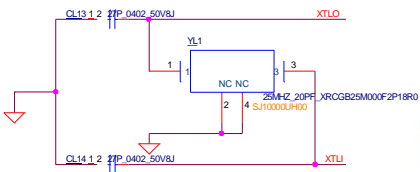
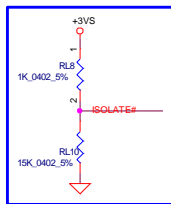
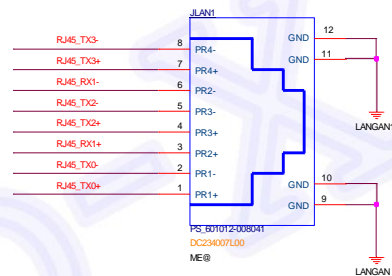




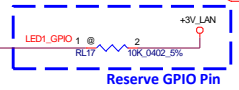
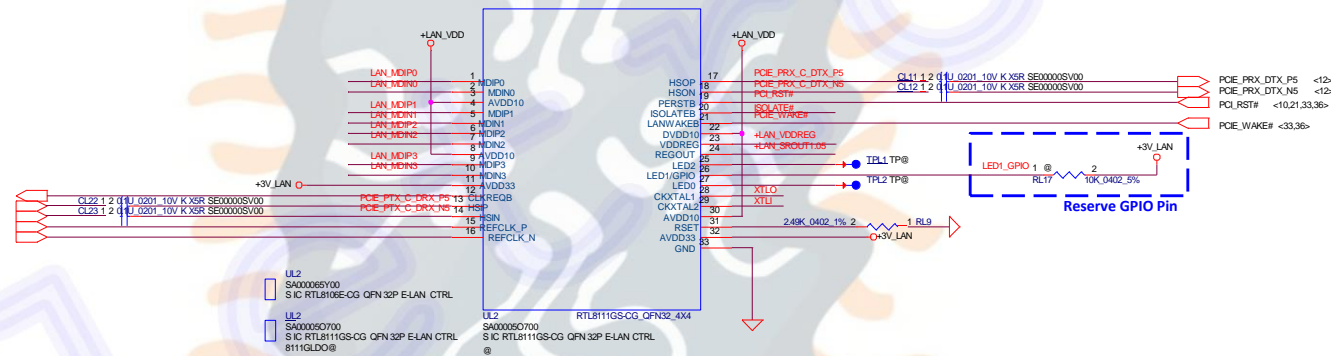
# LAN



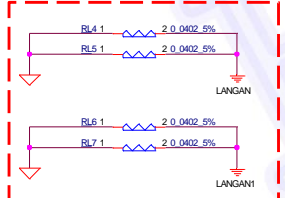
## RJ-45 Connector



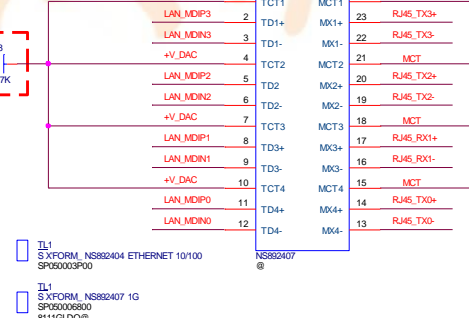
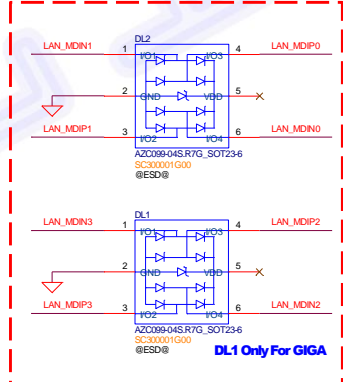
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<10> CLK\_POE\_LAN#



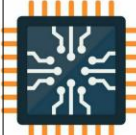
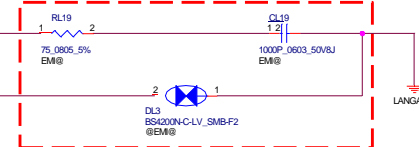
## EMI



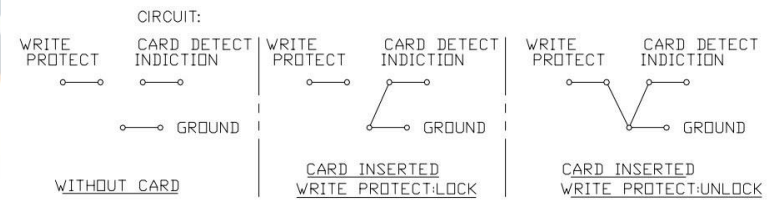
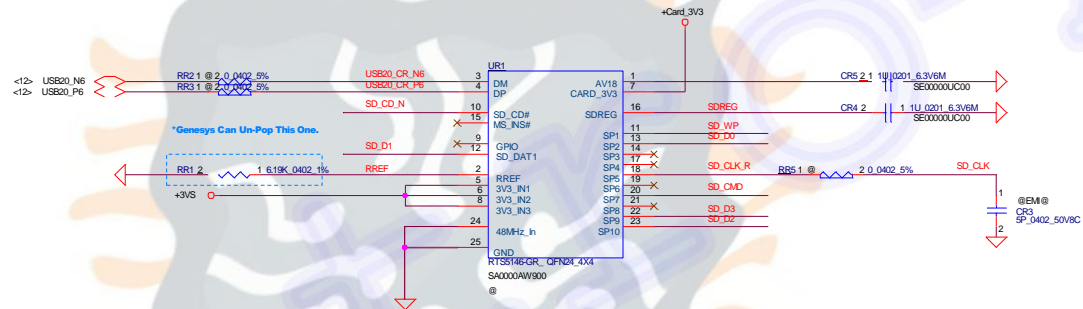
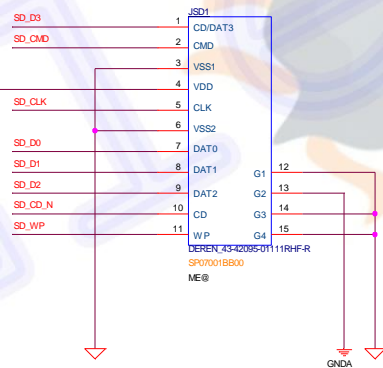
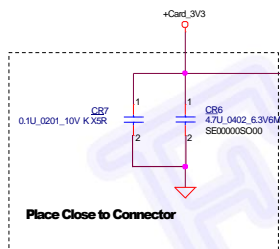
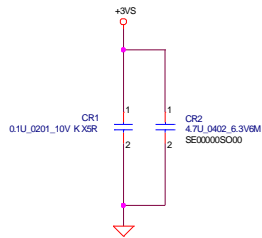
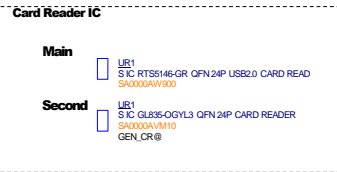
## ESD



## EMI



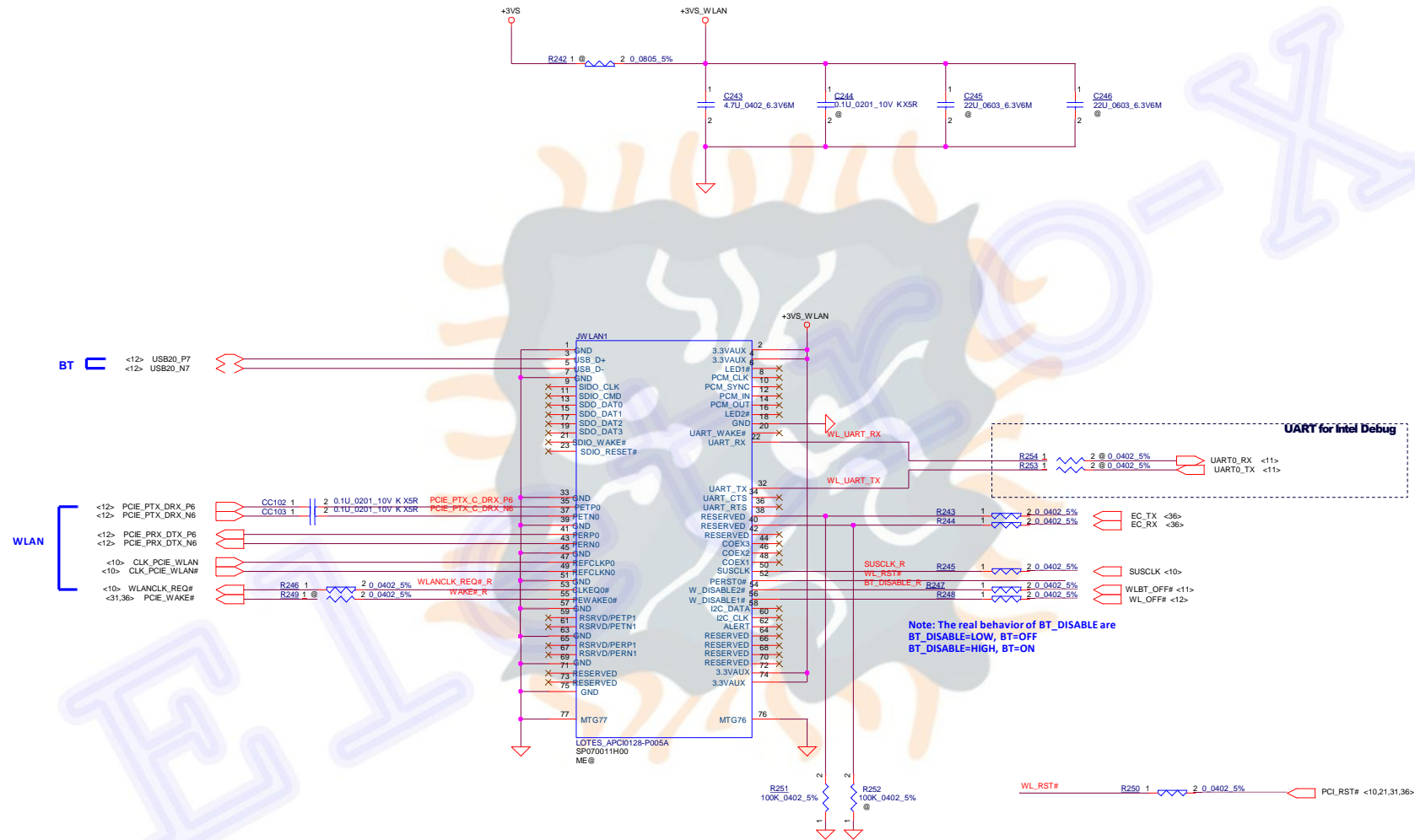
# CARD READER



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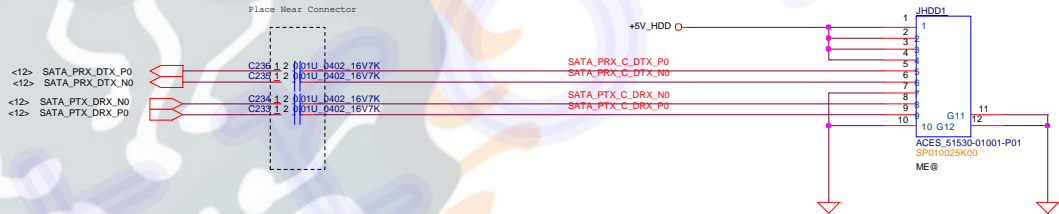
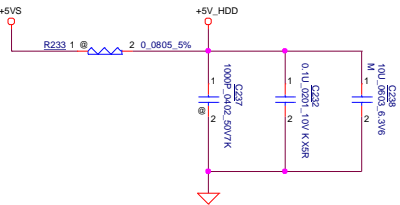


# NGFF - WLAN / BT (E- KEY)

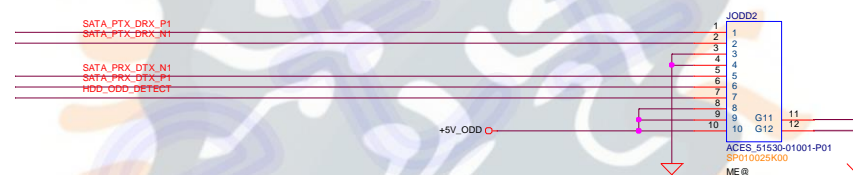
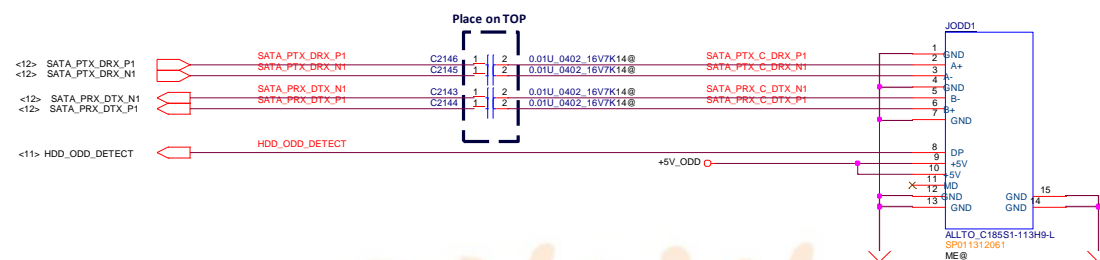




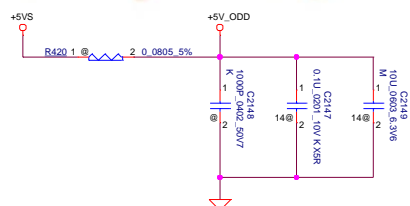
# HDD FFC Connector to Sub Board



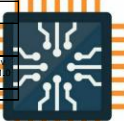
## ODD FFC Connector to Sub Board (15" Only)



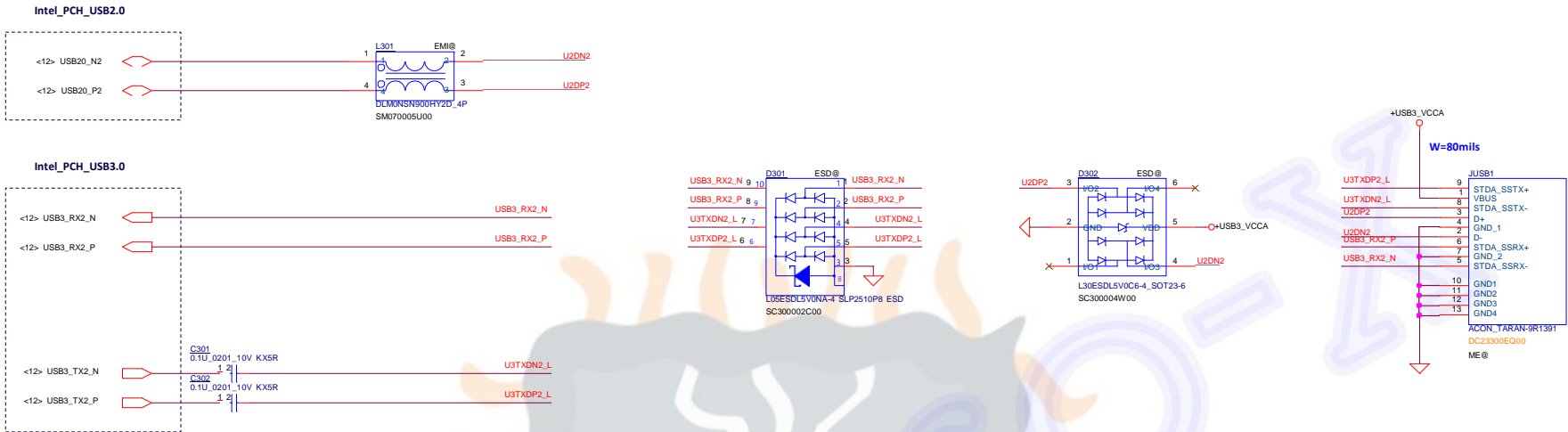
## ODD MISC.



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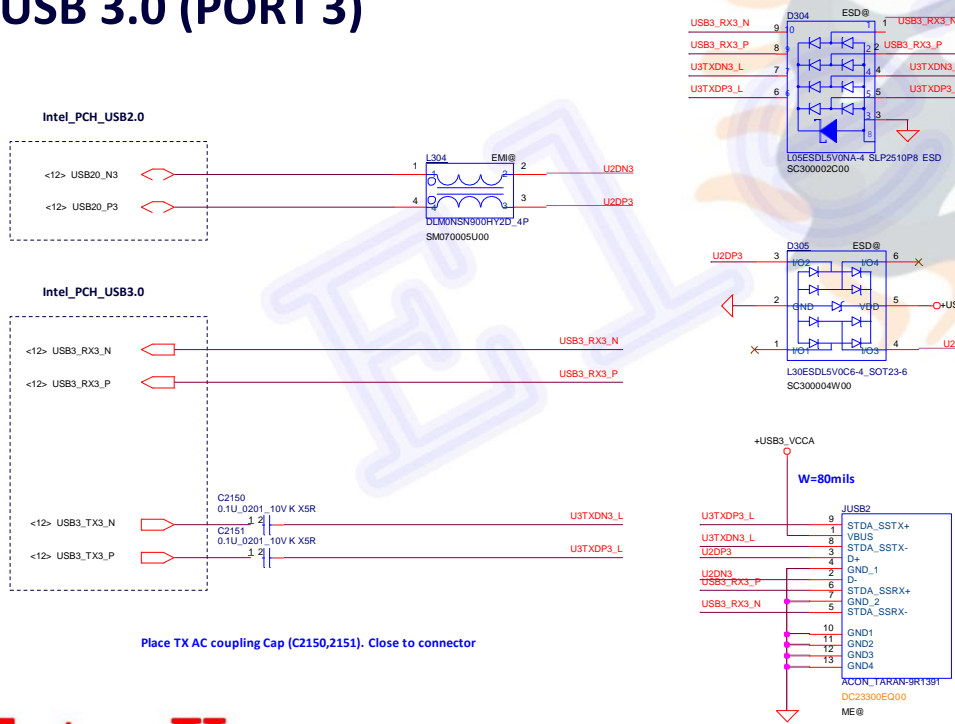


USB 3.0 (PORT 2)



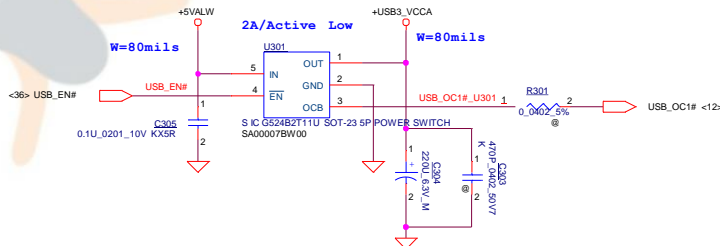
Place TX AC coupling Cap (C172,173). Close to connector

USB 3.0 (PORT 3)



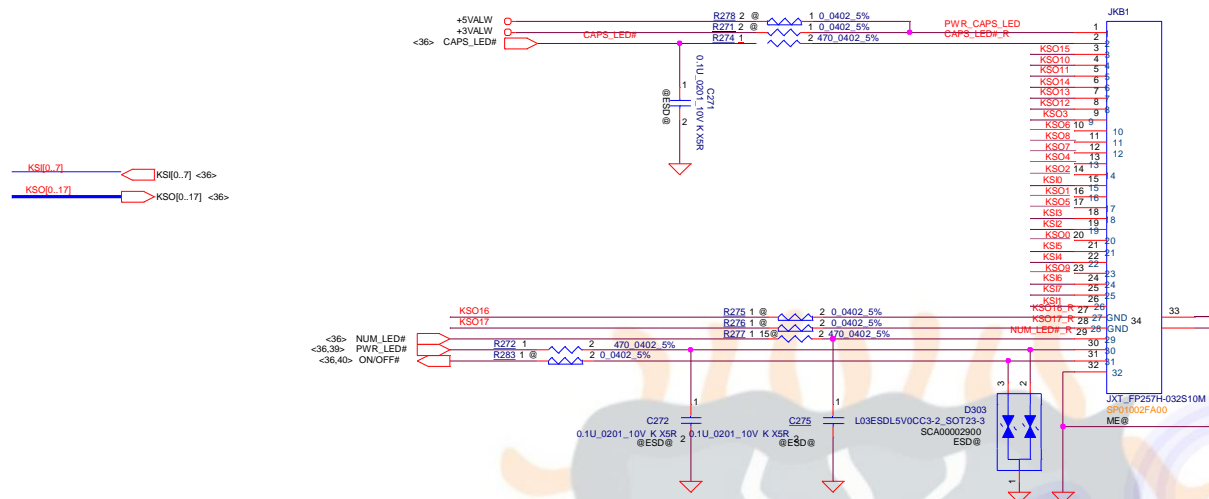
Place TX AC coupling Cap (C2150,2151). Close to connector

USB 3.0 MISC.

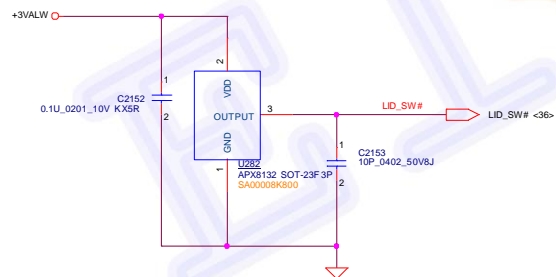




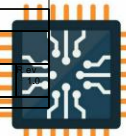
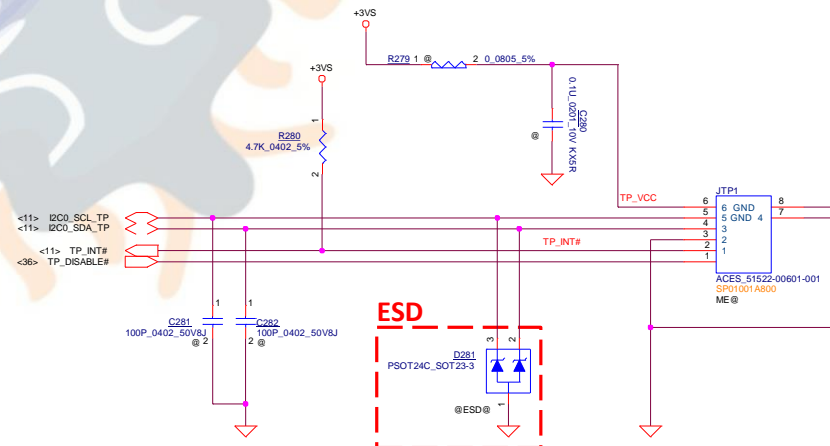
# KEYBOARD



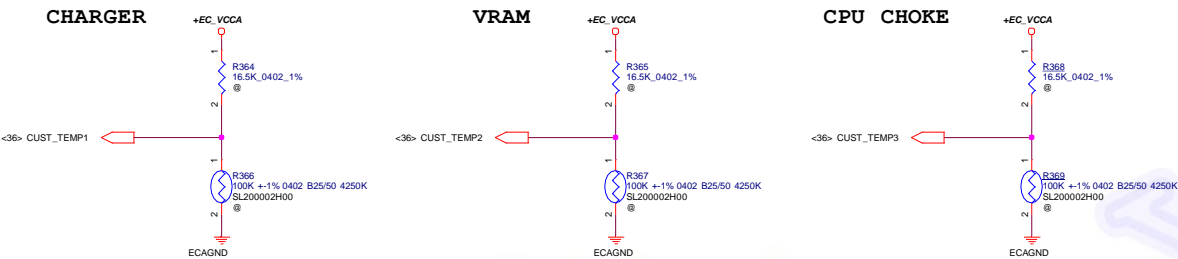
# HALL SENSOR



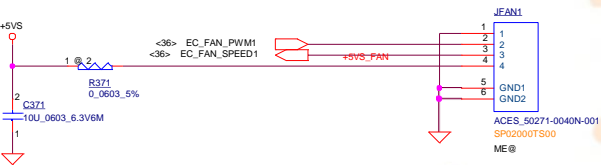
# TOUCH PAD



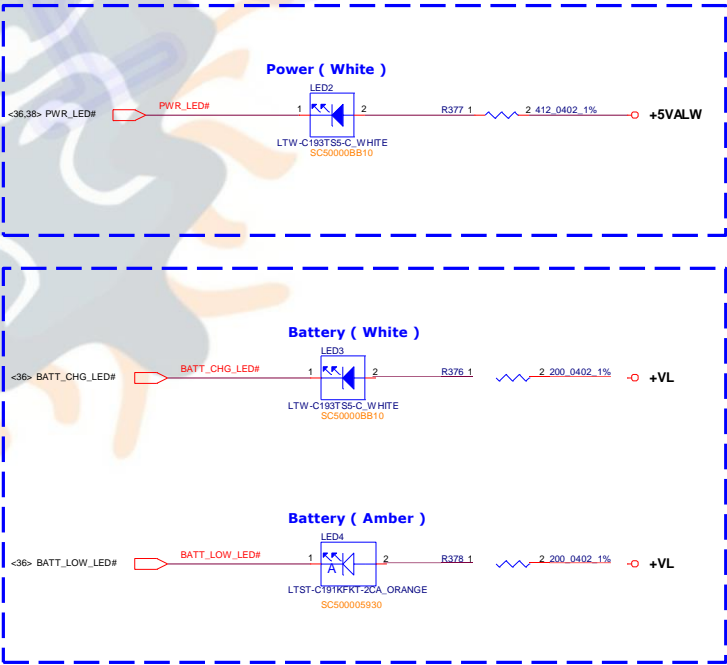
THERMISTOR



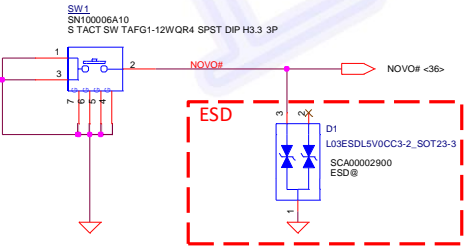
FAN



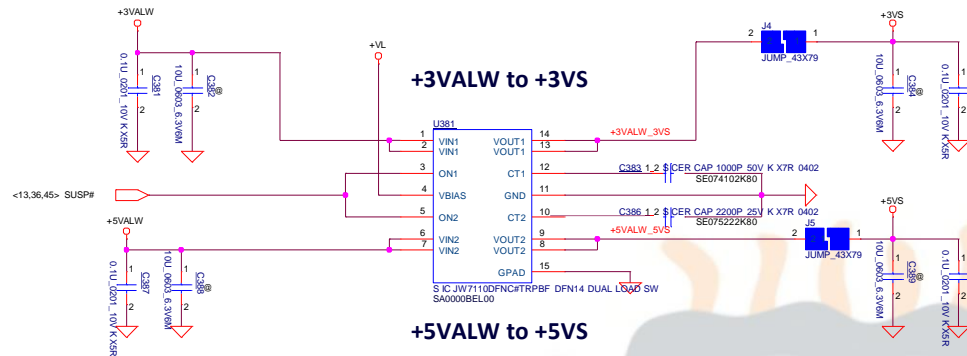
LED



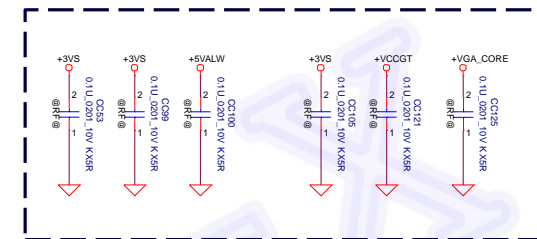
NOVO BUTTON



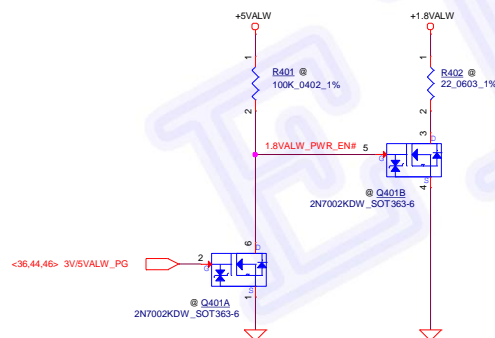
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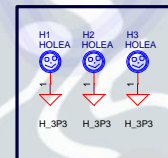
## RF By-Pass / Cross Moat Caps



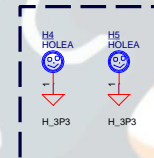
**For +1.8V<sub>ALW</sub> Discharge**



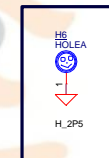
CPU



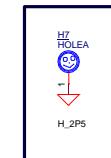
VGA



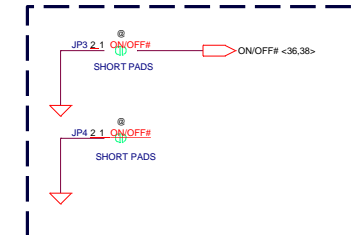
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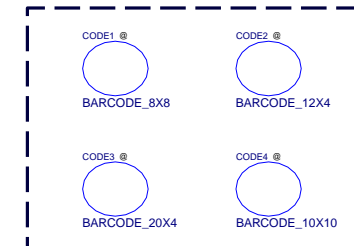
## BATTERY



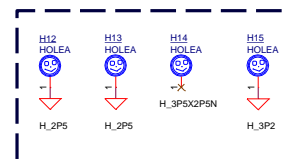
## ON/OFF# SHORT PADS



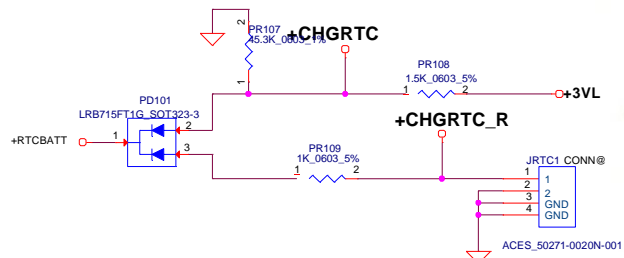
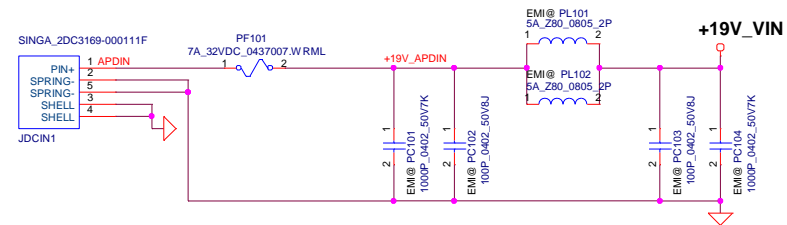
**LASER BARCODE**



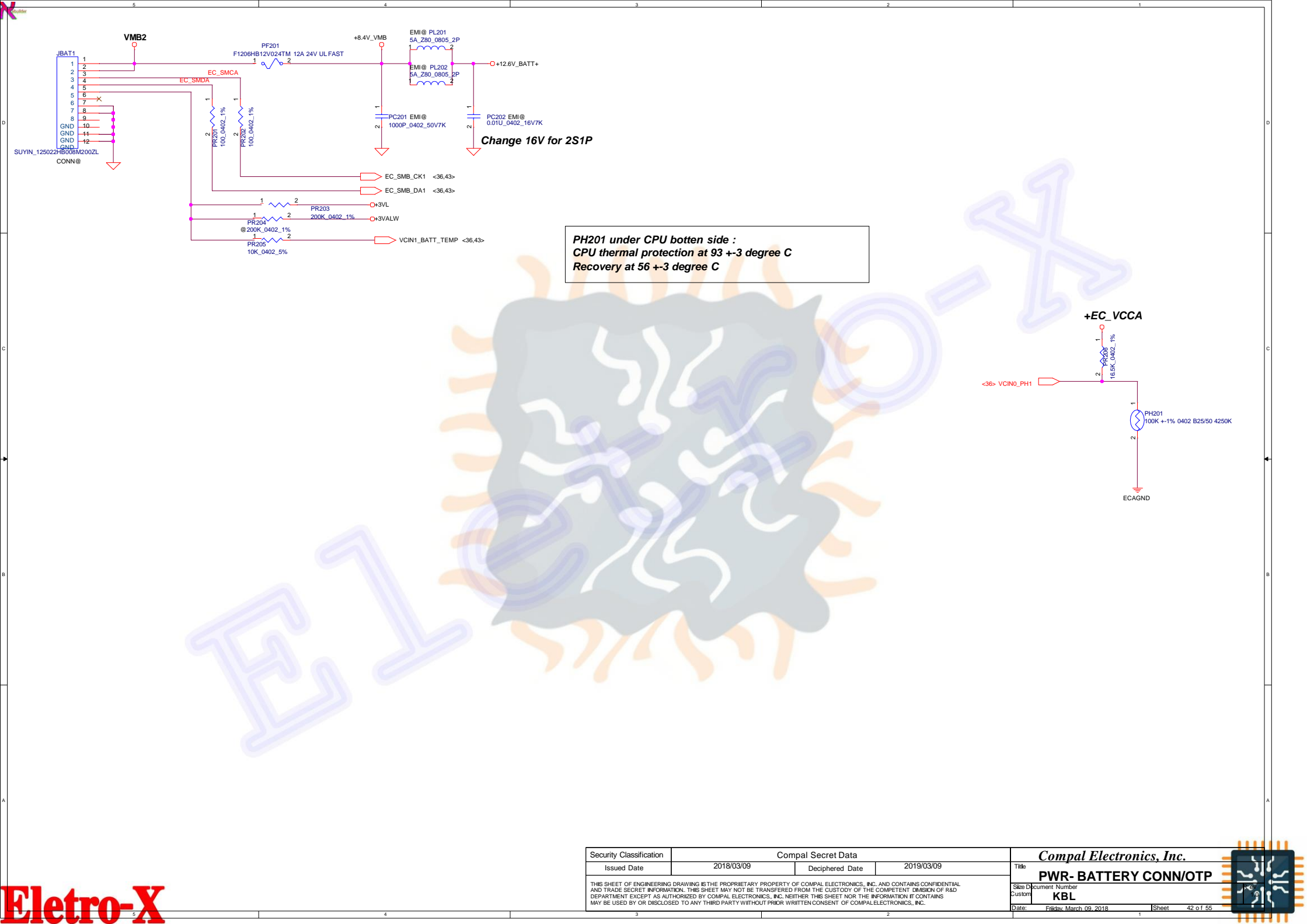
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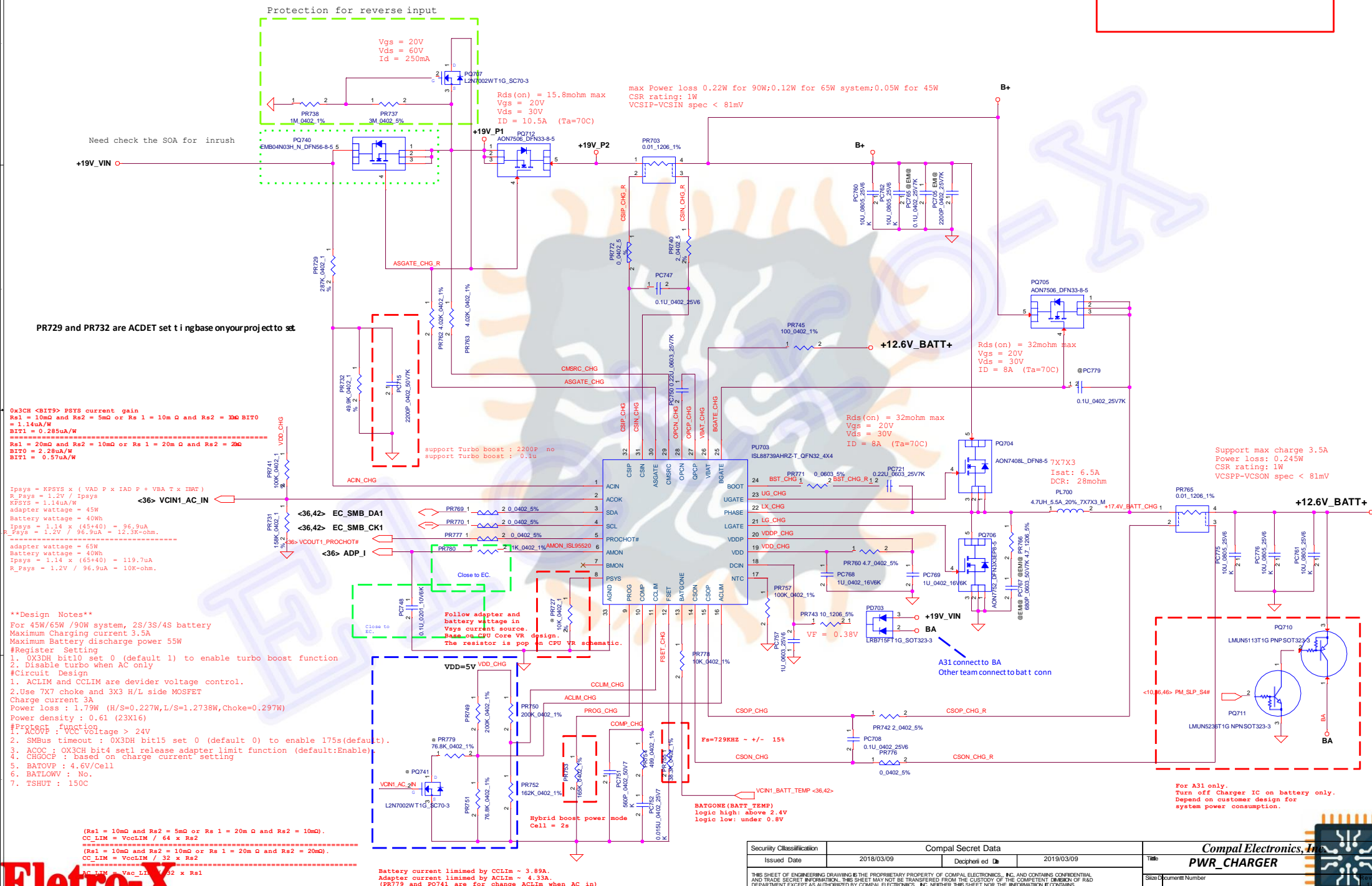


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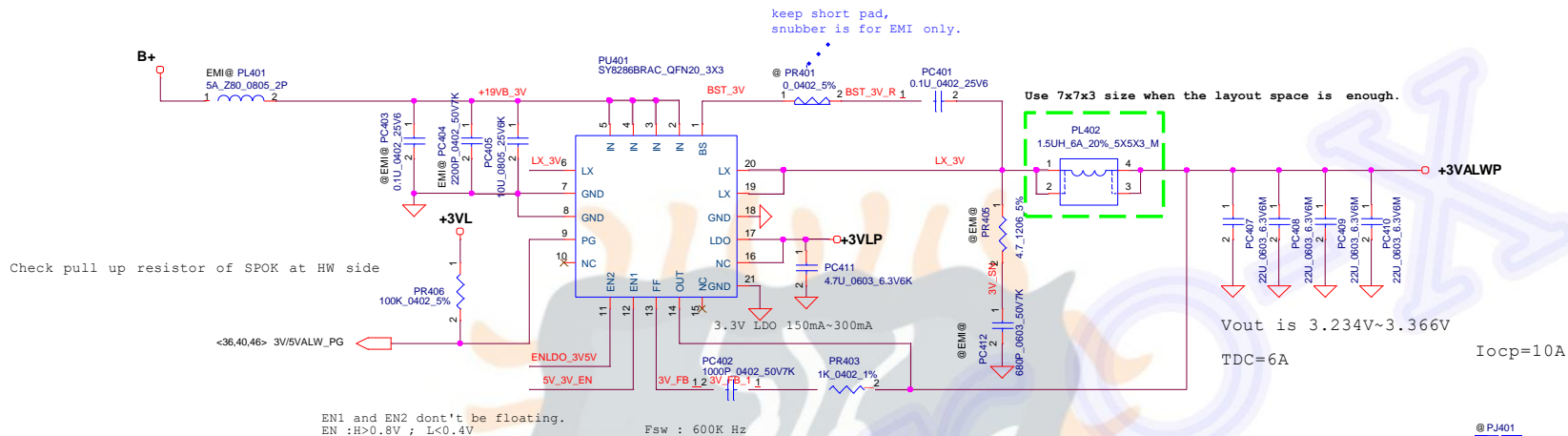






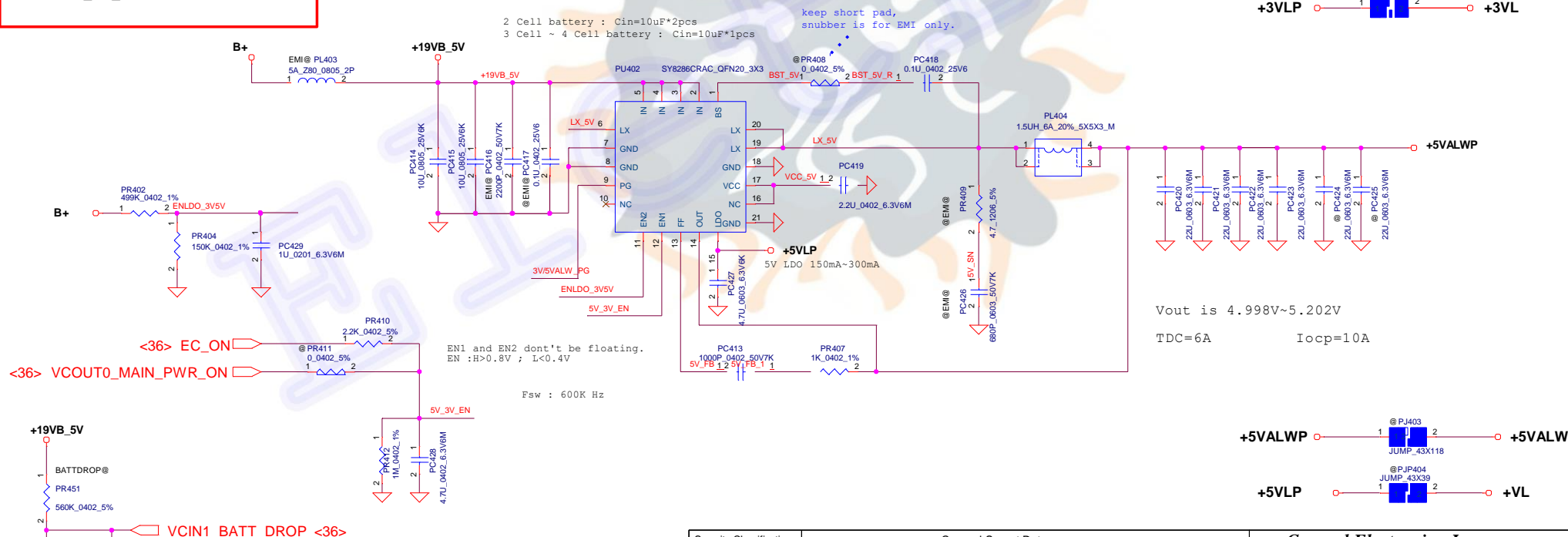
# Module model information

SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd



# Module model information

SY8286C\_V3\_single.mdd  
SY8286C\_V3\_dual.mdd

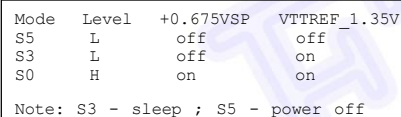


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RT8207P_single_V3.mdd	For Single layer
RT8207P_dual_V3.mdd	For Dual layer

RT8207P_single_V3.mdd	For Single layer
RT8207P_dual_V3.mdd	For Dual layer

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



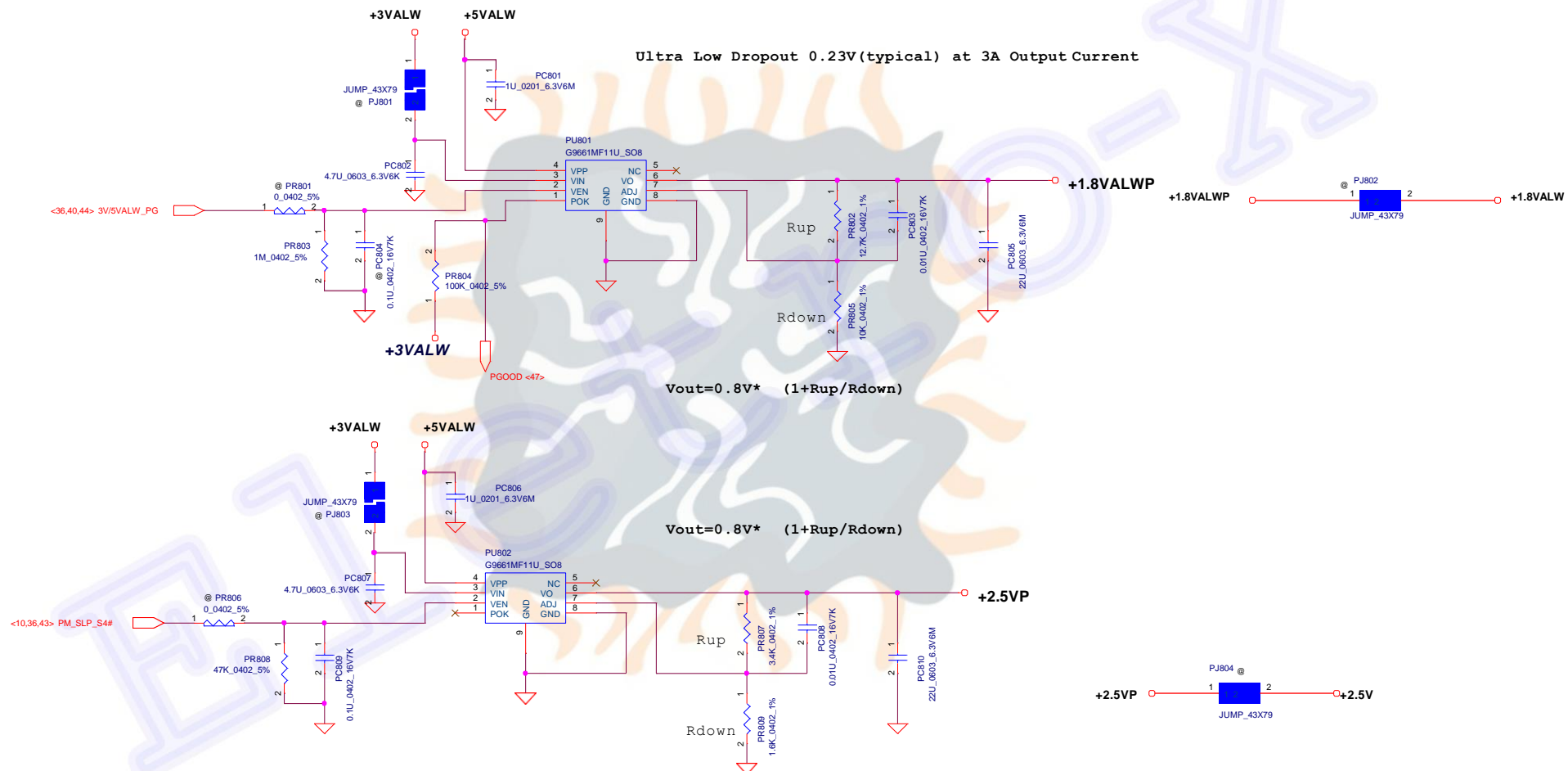
Switching Frequency: 540kHz  
Ipeak=8A  
Iocp~9.6A  
OVP: 113%~120%  
VFB=0.75V, Vout=1.3545V

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Title			
<b>RT8207P</b>			
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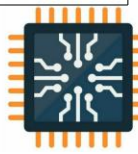


# Module model information

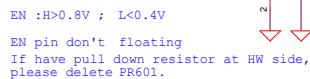
APL5930\_V2.mdd



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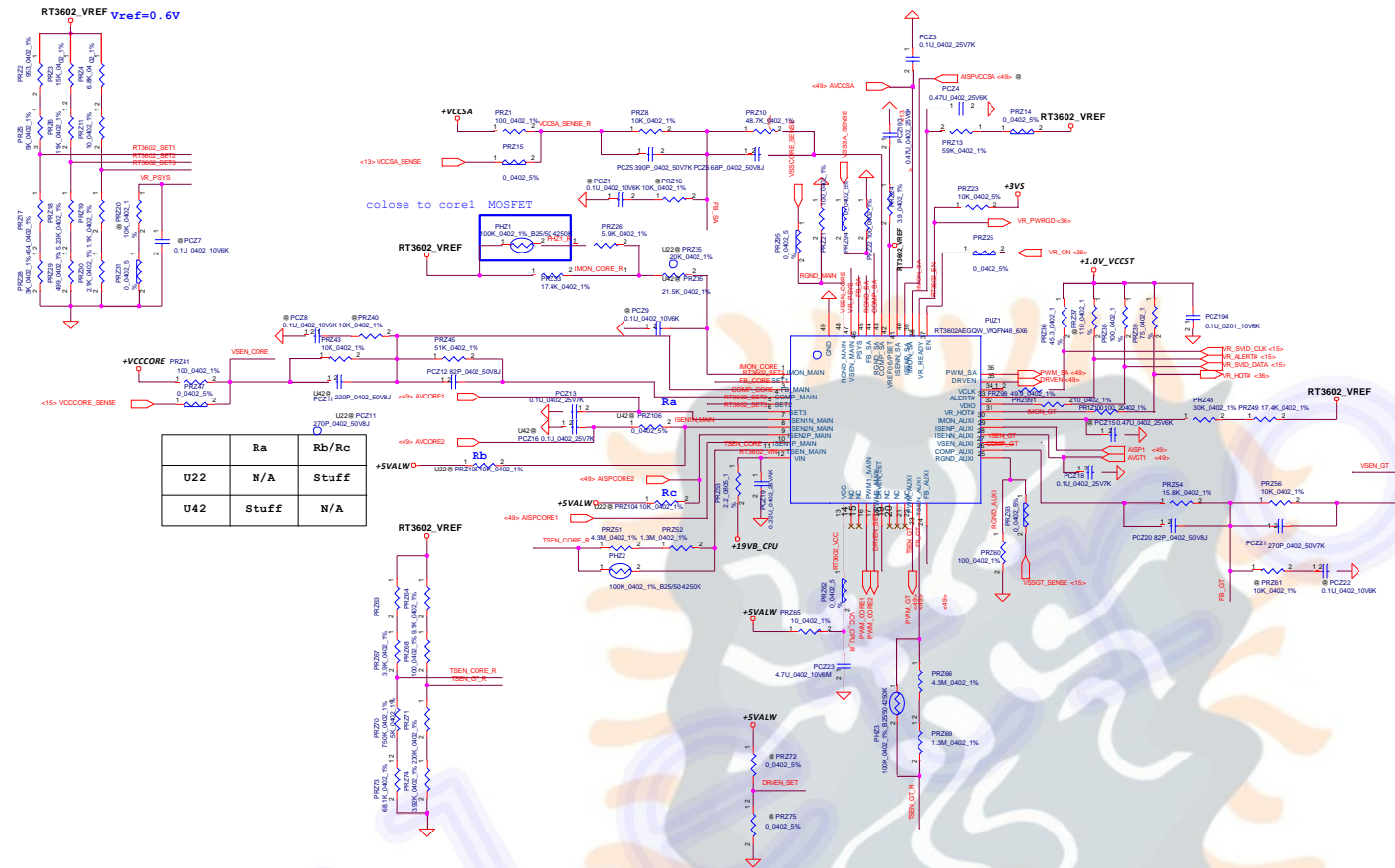


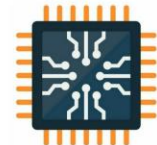
SY8286\_V2\_single.mdd  
SY8286\_V2\_dual.mdd



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

$$\begin{aligned} V_{out} &= 0.6V * (1 + R_1/R_2) \\ &= 0.6 * (1 + (14/20)) \\ V_{out} &= 1.02V \end{aligned}$$



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# PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefadj	PR8 39K	20K	39K
Rref1	PR7 39K	20K	30K
Rboot	PR10 1.5K	2K	3K
Rref2=PR20+PR21	PR20 30K	18K	24K
	PR21 1.5K	0	3K
C	PC9 1.5nf	2.7nf	1.8nf

Current Limit threshold setting  
 $Rocset = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10\mu\text{A}$

$I_{ripple} = (19 - 0.9) * 0.9 / (304.89 \text{ Khz} * 0.36\mu\text{s} * 19) = 7.811 \text{ A}$

$I_{ocp} = 42 \text{ A per phase}$   
 $I_{valley} = 42 \text{ A} - 7.811 \text{ A} / 2 = 38.0945 \text{ A}$

Choke: 0.22uH (Size: 10\*10\*4)  
 $R_{dc} = 0.82 \pm 5\%$   
Heat Rating Current=40A  
Saturation Current=90A  
 $C = 3 * 330\mu\text{F} (9\text{mohm}) = 990\mu\text{F}$   
 $V_{ripple} = \text{ripple} * \text{ESR}(\text{min}) = 7.811 \text{ A} * 3\text{mohm} = 23.4 \text{ mV}$

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

# Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14M-LP	N14P-LP
	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	13W	18.9W
Boosted GPU Total at Tj=102C	25W	20W	23W
EDP-Continuous at Tj=102C	24A	22A	25A
EDP-Peak at Tj=102C	35A	35A	35A
Istep max (Evaluation)	15A	20A	14A
OCP Setting Current	42A	42A	42A
Rocset (PR12)	10.2K	10.2K	10.2K
Recommendation	1phase 2H2L	1phase 2H2L	1phase 2H2L
PolymerCap (330uF)	6mohm * 2	6mohm * 2	6mohm * 2
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3

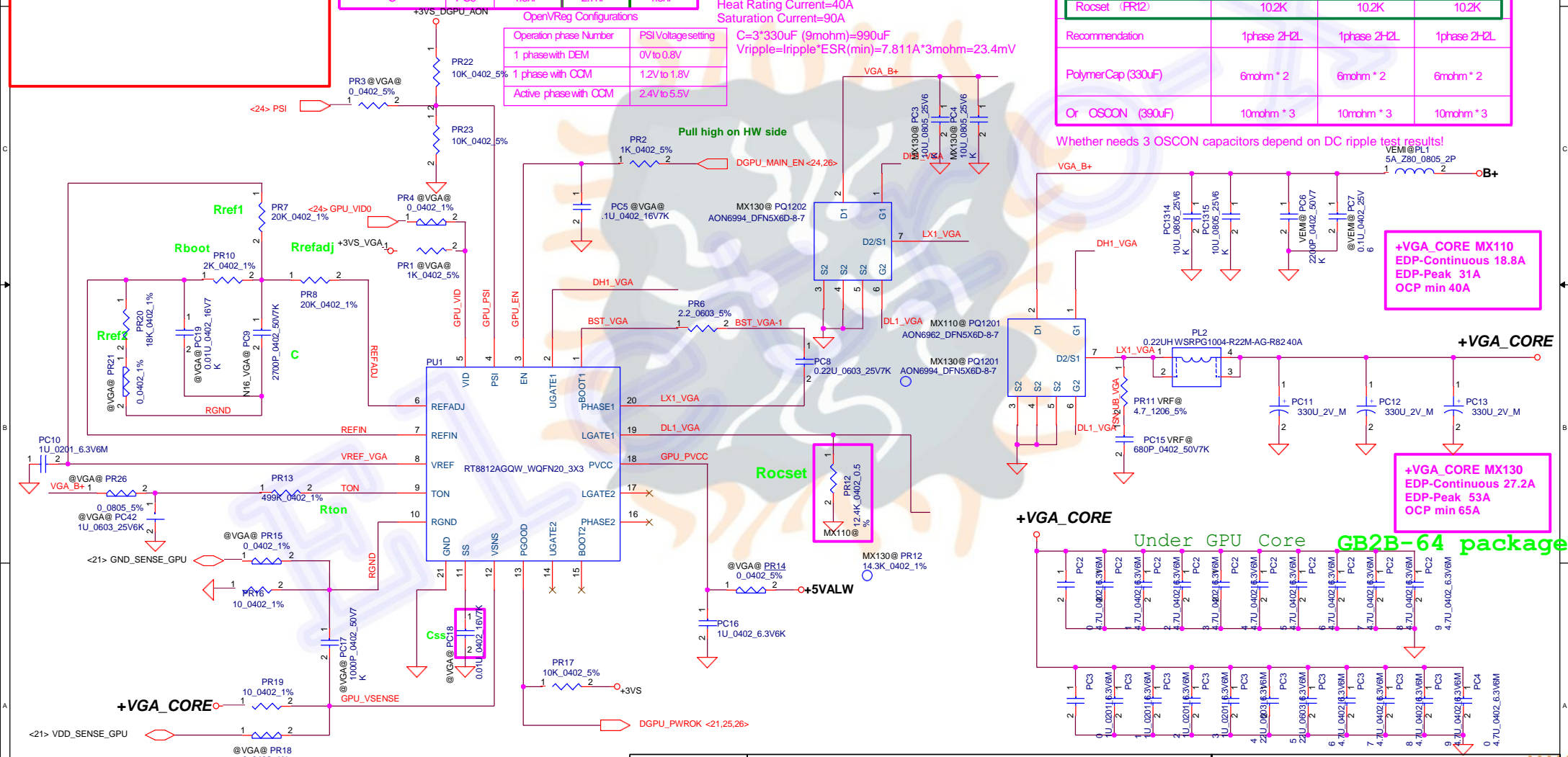
Whether needs 3 OSCON capacitors depend on DC ripple test results!

+VGA\_CORE MX110  
EDP-Continuous 18.8A  
EDP-Peak 31A  
OCP min 40A

+VGA\_CORE MX130  
EDP-Continuous 27.2A  
EDP-Peak 53A  
OCP min 65A

Under GPU Core GB2B-64 package

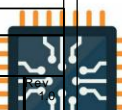
Module model information  
RT8812A-1P\_V2A.mdd for IC portion  
RT8812A-1P\_V2B.mdd for SW portion



Remark:  
1. Switching frequency setting:  $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3 \text{ ms}$   
 $I_{ss} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton}) = 0.01 \text{ U} * 0.9 \text{ V} / 5\mu\text{A} + 2.3 \text{ ms} = 4.1 \text{ ms}$  (PC18 pop)  
2. Soft-Start time (Internal) is 0.7ms (PC18 un-pop)

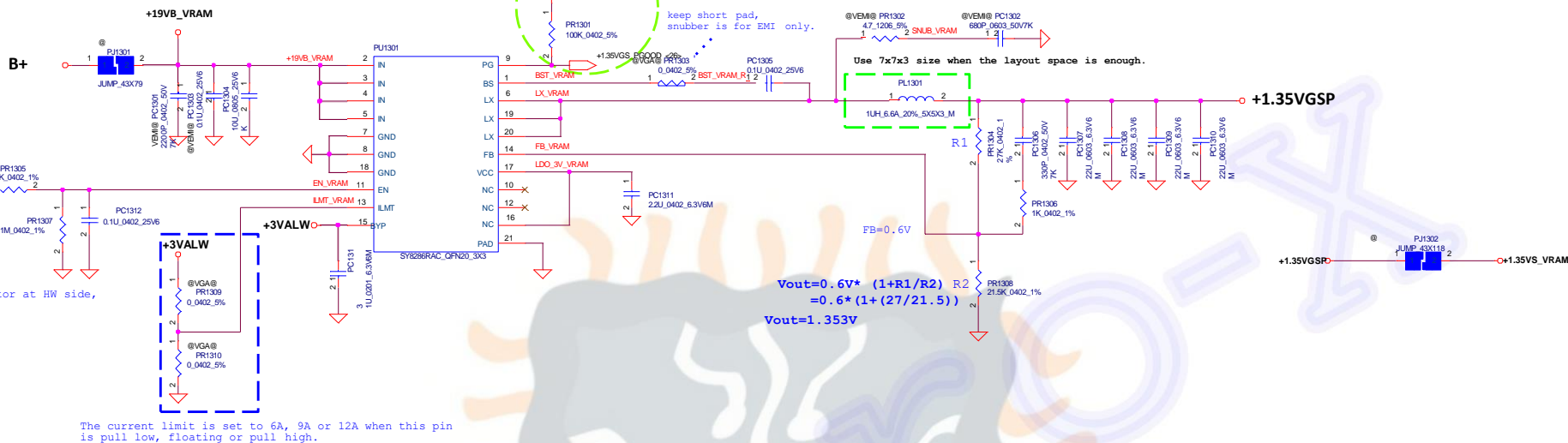
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VGA_CORE		VGA_CORE	
Size/Document Number		Custom	
Date:		Friday, March 09, 2018	
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# Module model information

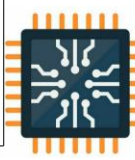
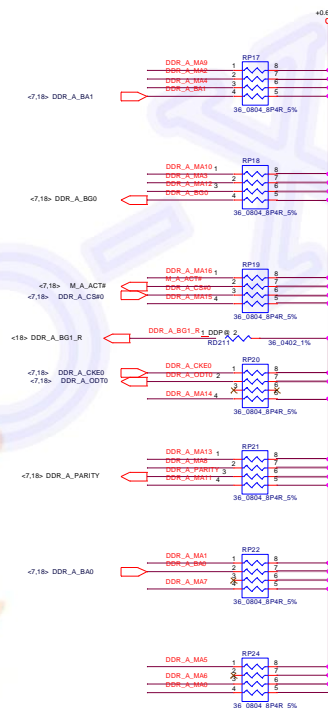
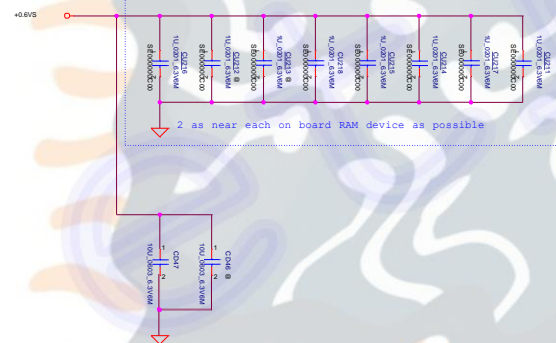
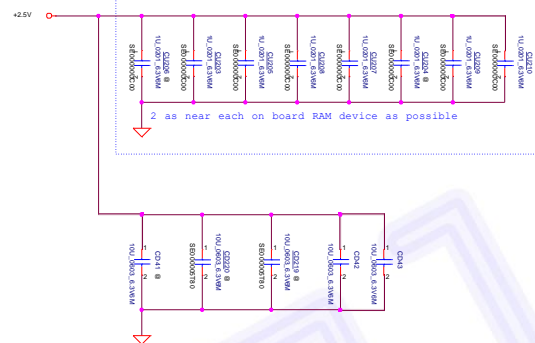
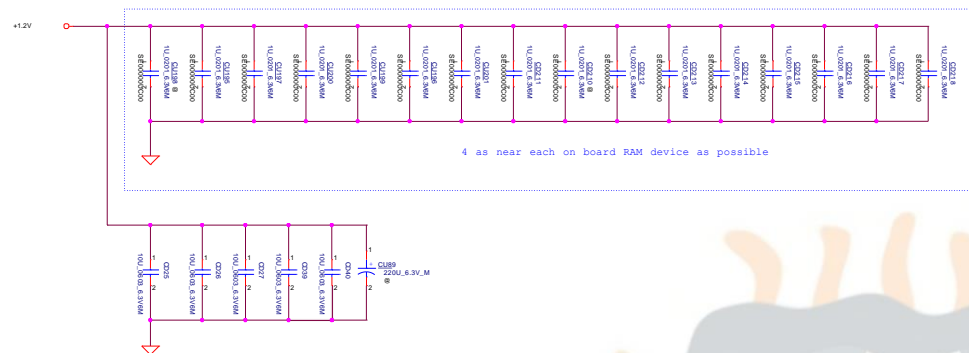
SY8286\_V2\_single.mdd  
SY8286\_V2\_dual.mdd



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				C	Rev 1.0
				Date: Feb 05, March 05, 2018	Sheet 52 of 55

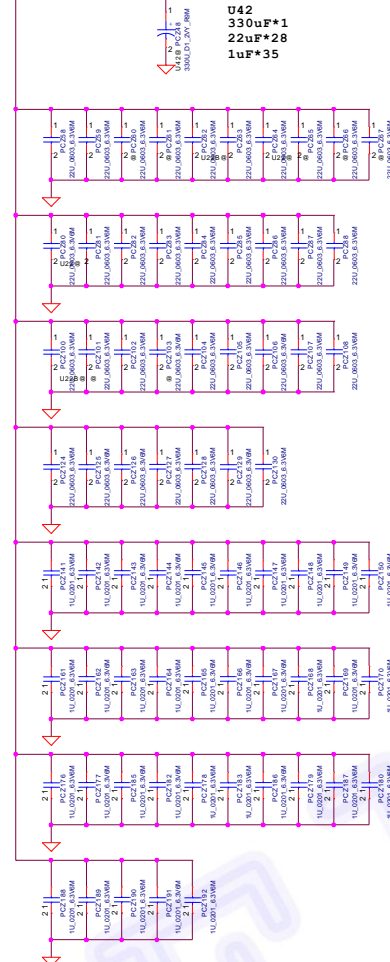


<7.1b> DDR\_A\_MA0[0..16]



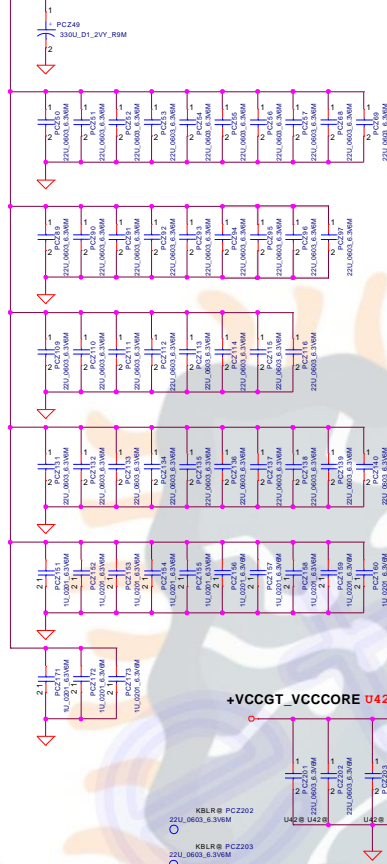
+VCCCORE

VCCCORE :  
U22  
22uF\*28  
1uF\*35  
U42  
330uF\*1  
22uF\*28  
1uF\*35



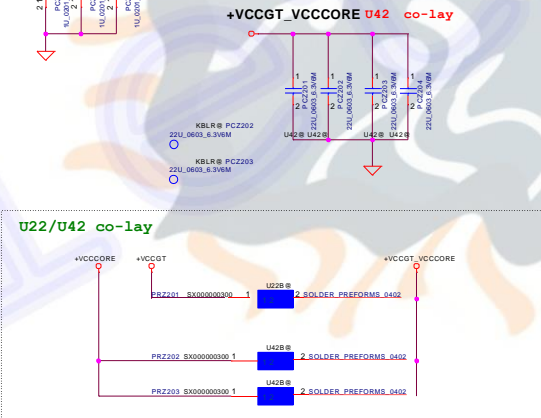
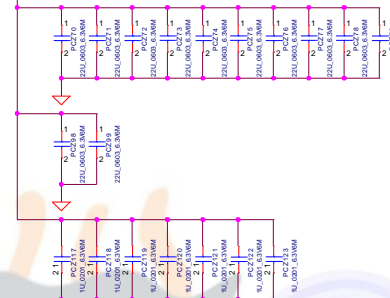
+VCCGT

VCCGT :  
U22 & U42  
330uF\*1  
22uF\*33  
1uF\*13



+VCCSA

VCCSA :  
U22 & U42  
22uF\*9  
1uF\*7



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Date: 1986, March 28, 2018				Sheet 50 of 55





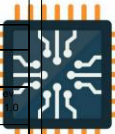
## Version change list (P.I.R. List)

Page 1 of 1  
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Down size for material shortage	P49	Change PRA6,PRA9,PRG6 from 1K +-1% 0603 to 1K +-1% 0402	2018.03.05	SVT
2	Down size for material shortage	P49	Change PRZ102,PRZ85 from 1.2K +-1% 0603 to 1.2K +-1% 0402	2018.03.05	SVT
3	Down size for material shortage(U42 SKU)	P49	Change PRZ103,PRZ87 from 1.2K +-1% 0603 to 1.2K +-1% 0402	2018.03.05	SVT
4	Down size for material shortage	P49	Change PRG9 from 2.05K +-1% 0603 to 2.05K +-1% 0402	2018.03.05	SVT
5	Down size for material shortage	P43	Change PR404 from 499K +-1% 0402 to 150K +-1% 0402 Change PC429 from 1U 16V K X5R 0402 to 1U 6.3V M X5R 0201	2018.03.05	SVT
6	Down size for material shortage	P50 P51	Change PC10,PC1313,PC30,PC31,PC32,PC33,PC614,PC801,PC806,PCZ117,PCZ151, PCZ166,PCZ167,PCZ170,PCZ179 from 1U 6.3V K X5R 0402 to 1U 6.3V M X5R 0201	2018.03.05	SVT
7	Down size for material shortage	P49	Change PCA1,PCG1,PCZ40,PCZ41 from 2.2U 16V K X5R 0402 to 2.2U 6.3V M X5R 0402	2018.03.05	SVT
8	Change size for common design	P44	Change PC401,PC418,PC603,PC1305 from 0.1U 10V K X5R 0201 to 0.1U 25V K X5R 0402	2018.03.05	SVT
9	Down size for material shortage	P48	Change PCZ23 from 4.7U 10V K X5R 0603 to S CER CAP 4.7U 10V M X5R 0402	2018.03.05	SVT
10	Down size for material shortage	P51	Change PC20,PC28,PC36,PC37,PC38,PC39,PC40 from 4.7U 6.3V K X5R 0603 to 4.7U 6.3V M X5R 0402	2018.03.05	SVT
11	Down size for material shortage	P45	Change PC505 from CAP .1U 25V K X7R 0603 to 0.1U 25V K X7R 0402	2018.03.05	SVT
16					
17					

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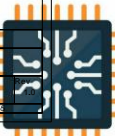
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Title PIR (PWR)	
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Version change list  
(P.I.R. List)Page 1 of 2 for  
HW

Item	Reason for change	PG#	Modify List	Date	Phase
1	ME Request	41	Add Screw Hole H15.	2017/12/13	EVT -> PVT
2	ME Request	41	Remove Screw Hole H16.	2017/12/15	EVT -> PVT
3	0 Ohm Reduction	31	Replace RA2 with R-Short.	2017/12/18	EVT -> PVT
4	0 Ohm Reduction	34	Replace R242 with R-Short.	2017/12/18	EVT -> PVT
5	0 Ohm Reduction	29	Replace R203, R211, R212 with R-Short.	2017/12/18	EVT -> PVT
6	Phase Out Un-Necessary X4E Level	3	Remove X4EABQ38L51 and X4EABQ38L52.	2017/12/19	EVT -> PVT
7	Update 14" PCB DA Part Number.	3	DA6001Y6000 -> DA6001Y6100	2017/12/19	EVT -> PVT
8	Cost Down Plan	36	C2147, C2149 -> 14" Only (BOM Structure Modify)	2017/12/20	EVT -> PVT
9	0 Ohm Reduction	36	Replace R420 with R-Short.	2017/12/20	EVT -> PVT
10	Cost Down Plan	20	Un-Pop CU206, CU204, CD41, CU198, CD210, CU213, CU212, CD46	2017/12/21	EVT -> PVT
11	Cost Down Plan	19	Un-Pop C2140, CD19, CD10, CD32, CB33, CD23	2017/12/21	EVT -> PVT
12	Cost Down Plan	18	Un-Pop CD127	2017/12/21	EVT -> PVT
13	Cost Down Plan	13	Replace CC45 with 10uF	2017/12/21	EVT -> PVT
14	0 Ohm Reduction	35	Replace R233 with R-Short.	2017/12/21	EVT -> PVT
15	0 Ohm Reduction	39	Replace R275, R276, R277, R279 with R-Short.	2017/12/21	EVT -> PVT
16	0 Ohm Reduction	10	Replace RC103 with R-Short.	2017/12/21	EVT -> PVT
17	0 Ohm Reduction	19	Replace RD108, RD140 with R-Short.	2017/12/21	EVT -> PVT
18	0 Ohm Reduction	39	Replace R283 with R-Short.	2017/12/21	EVT -> PVT
19	0 Ohm Reduction	37	Replace R425, R428, R102 with R-Short.	2017/12/21	EVT -> PVT
20	0 Ohm Reduction	32	Replace RL18 with R-Short.	2017/12/21	EVT -> PVT
21	0 Ohm Reduction	40	Replace R371 with R-Short.	2017/12/21	EVT -> PVT
22	Cost Down Plan	28	Un-Pop CV703, CV707, CV708, CV718 (DIS@)	2017/12/21	EVT -> PVT
23	Cost Down Plan	27	Un-Pop CV603, CV607, CV614, CV616, CV617 (DIS@)	2017/12/21	EVT -> PVT
24	Cost Down Plan	22	Un-Pop CV35 (DIS@)	2017/12/21	EVT -> PVT
25	Cost Down Plan	28	Replace CV701 with 10uF	2017/12/21	EVT -> PVT
26	Cost Down Plan	27	Replace CV602 with 10uF	2017/12/21	EVT -> PVT
27	Cost Down Plan	41	Un-Pop Q401, R401, R402	2017/12/21	EVT -> PVT
28	Cost Down Plan	13	Un-Pop CC40	2017/12/21	EVT -> PVT
29	Cost Down Plan	18	Replace RD200, RD201, RD202, RD203, RD205 with R-Short. (SDP@/BDP@)	2017/12/21	EVT -> PVT
30	Cost Down Plan	20	RD211 -> DDP Only (BOM Structure Modify)	2017/12/21	EVT -> PVT
31	VRAM EOL	27, 28	Remove VRAM UV8, UV9 (Replace with x32 DIE *2)	2017/12/22	EVT -> PVT

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